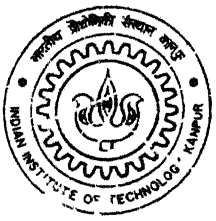
A STUDY INTO THE APPLICABILITY OF P^+N^+ UNIVERSAL CONTACT TO POWER SEMICONDUCTOR DIODES AND TRANSISTORS FOR FASTER REVERSE RECOVERY

By

RAGHUBIR SINGH ANAND



DEPARTMENT OF ELECTRICAL ENGINEERING

INDIAN INSTITUTE OF TECHNOLOGY KANPUR

July 2001

A STUDY INTO THE APPLICABILITY OF P^+N^+ UNIVERSAL CONTACT TO POWER SEMICONDUCTOR DIODES AND TRANSISTORS FOR FASTER REVERSE RECOVERY

A Thesis Submitted
In Partial Fulfillment of the Requirements
For the Degree of

DOCTOR OF PHILOSOPHY

By

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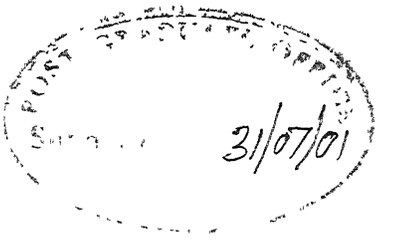
to the

DEPARTMENT OF ELECTRICAL ENGINEERING

INDIAN INSTITUTE OF TECHNOLOGY KANPUR

July 2001

CERTIFICATE



This is to certify that the work contained in the thesis entitled "A Study into the Applicability of P^+N^+ Universal Contact to Power Semiconductor Diodes and Transistors for Faster Reverse Recovery" by Raghubir Singh Anand has been carried out under our supervision and this work has not been submitted elsewhere for a degree.

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To

MY FATHER

in memoriam

ACKNOWLEDGEMENT

I express my deep gratitude and thanks to my thesis supervisors Dr Jitendra Narain and Dr Baquer Mazhari for their active participation, constant guidance, ablest supervision and moral support during this dissertation work

I express my deep sense of gratitude towards Prof. SC Srivastava, Head EE Department and Prof. R. Sharan, Head Samtel Center, IIT Kanpur for their constant support and encouragement. I am thankful to Prof. KR Srivathsan, Ex-Head, EE Dept. to provide me computing facilities and space at telematic Lab.

I express my sincere thanks to the Director, officer and staff of IRDE, Dehra Dun for their co-operation and support during this endeavor.

I thank Mr. LS Gupta & Mr. RA Verma for providing technical support for the experimental part of the work I deeply acknowledge the co-operation extended by Mr. Vivek Mudgil, Ms Neeru Chhabra, Mr. Vineet Narain and others of the telematic group and Mrs Mudgil of VLSI/EDA facility. At this moment I remember all my old colleagues Mr. G. Swaminathan, Late Sangita Goel, Ms Bishakha, Dr Anjali, Ms Neelam and others who have worked with me in Semiconductor Device Lab, IIT, Kanpur and helped to maintain good working relations. I also appreciate the co-operation and assistance given by Dr Asha Awasthi and Mr. Anand Biswas during this period.

It is with the blessing of my parents, parents-in-laws, elders and well wishes of my sisters, sister-in-laws, brother-in-laws and dear ones that I have been able to complete the work of the present nature. Master Sumit and Navdeep, my sons managed their studies on their own. Hope they understand the commitments and compulsions of the assignment of the present nature. Last but not the least, my wife has given me full support and stood with me during the period when my spirits were down.

Raghubir Singh Anand

July, 2001.

Thesis Title: A STUDY INTO THE APPLICABILITY OF P^+N^+ (UNIVERSAL CONTACT) TO POWER SEMICONDUCTOR DIODES AND TRANSISTORS FOR FASTER REVERSE RECOVERY

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SYNOPSIS

PN junction diodes and Bipolar junction transistors (BJTs) are used in a wide variety of switching applications, such as, TV deflection circuits, motor drives, switched mode power supplies and others. In most of these applications, the diodes and transistors are used for operation at frequencies less than 100 kHz. The limiting mechanism for the speed of operation is the presence of stored minority charge during the ON state and the reverse recovery time required for removing these stored charges. The uni-polar devices like Schottky and MOS are inherently fast because of absence of minority charge storage but also have the disadvantage of lower reverse breakdown voltage and higher heat dissipation in comparison to bipolar devices. The Insulated Gate Bipolar Transistor (IGBT) has low on-state losses but due to its relatively involved technology, it is restricted to higher end devices. Even with the limitations as compared to Schottky,

MOSFET and IGBT, the PIN rectifiers and BJT are still used in various applications. There have been developments to enhance the switching performance of diodes and transistor, such as, through Au doping and through use of Schottky clamp transistor. In 1982, Amemiya [1] introduced a concept known as universal contact to improve reverse recovery performance of diodes and transistors. The present work is concerned with the various aspects of the application of the "universal contact" (UC) to diodes and transistors.

Amemiya et al showed that the incorporation of n^+p^+ UC in a p^-nn^+ diode at the n^+ end resulted in significant improvement in reverse recovery and decrease in the forward ON voltage. In addition, the application of UC had an advantage when compared to the technique of Au doping to control the reverse recovery, that it did not lead to increase of leakage current or a soft breakdown.

The incorporation of universal contact in the n^+ region such that it adjoins the lightly doped n region, works well with diodes of low or moderate breakdown voltage, but degrades the reverse blocking capability of high voltage diodes due to the onset of reach-through. Kitagawa [2] proposed the incorporation of p^+n^+ universal contact inside the diffused region of the p^+nn^+ diode away from the lightly doped region; this avoided the reach-through and still improved the reverse recovery time. Besides diodes, the universal contact has also been applied to low voltage BJTs to obtain significant reduction in storage time, Narain [3].

In the work [1-3], although the usefulness of the universal contact has been demonstrated, its application however has been in a limited range of current, voltage and devices. It will be further desirable to explore the effects of incorporation of UC over a

wider range of current and voltage in diodes and transistors and other devices. The application of UC in a diode or transistor involves creating new diffused regions in an otherwise conventional device. The presence of these new regions alters the distribution of minority carriers and the currents flowing within the device. It is necessary to have a suitable analysis and model, which can account for the various phenomenon taking place inside the device and their influence on various parameters of the device.

Keeping in view the above considerations, we define the following objectives of the thesis -

(1) To study the reduction in reverse recovery due to incorporation of universal contact and its effects on other device characteristics using a combination of analytical modeling, numerical simulation, fabrication and characterization of low and high voltage PIN diodes with and without incorporating of universal contact.

(2) To suggest changes in the design of PIN diode to achieve better characteristics.

(3) 3To study and model the reduction in reverse recovery due to incorporation of UC and its effects on other device characteristics using a combination of analytical modeling, numerical simulation, fabrication and characterization of low and high voltage BJT with and without incorporating universal contact.

(4) To suggest changes in design of BJT to achieve better characteristics.

The major contributions of this thesis are:

1. A theoretical framework is developed which shows that effective minority carrier lifetime (τ_{eff}), defined as the ratio of total minority charge stored to the total current flowing through the diode, can be viewed as a function of three time constants: $\tau_{eff}^{-1} = \tau_L^{-1} + \tau_M^{-1} + \tau_R^{-1}$, where $\tau_L/\tau_M = I_M/I_L$, τ_M is the recombination lifetime in the lightly doped middle region and $\tau_R/\tau_M = I_M/I_R$. I_L, I_R and I_M are the minority carrier currents injected into the left p^+, right n^+ and middle ν regions Using this viewpoint, it is shown that effective minority carrier lifetime and therefore reverse recovery time which is closely related to it, can be reduced by redistributing current away from lightly doped ν-region to n^+ and p^+ regions where effective minority carrier lifetime can be reduced by incorporating universal contact.

2. The analytical model developed in this work shows that the effective lifetime decreases with increase in current density and that the advantages of incorporating a universal contact decrease as the breakdown voltage of the diode increases. It is also shown that the incorporation of universal contact allows a new tradeoff between the switching speed and the reverse blocking voltage determined by the proximity of universal contact to the lightly doped region of the diode. The predictions of the model are verified through extensive 2-D [4] numerical simulation and fabrication and characterization of low (~150 V) and high (>1000 V) voltage diodes. [5]

3. A new diode structure incorporating universal contacts inside both n^+ and p^+ diffused regions is proposed. It is shown through analytical calculations and 2D numerical simulations that this diode structure results in large reduction in reverse recovery. The improvements in reverse recovery are 60% and 66% at 0.3 A/cm^2 and 50 A/cm^2 respectively with respect to the conventional diode structure.

4. The analytical model developed for PIN diodes is extended to model the effects of incorporating universal contact within the extrinsic base of BJTs. It is shown that the use of universal contact allows redistribution of base current in saturation from collector region where recombination lifetime is high to extrinsic base region where effective recombination lifetime is low. As for the diode case, the model predicts improvement in switching speed with increase in collector current density but degradation of switching characteristics with increase in transistor's reverse blocking voltage. These results are verified through 2-D numerical simulation

5. The improvement in switching characteristics as a result of incorporation of universal contact is accompanied with an increase in the ON state voltage, $V_{CE(sat)}$ of transistors. The increase in $V_{CE(sat)}$ in transistors with UC is attributed to decrease of β_R, the reverse current gain and early onset of quasi-saturation effects

6. The usefulness of the universal contact in high voltage (BV_{CBO} >1000 V) transistors has been experimentally demonstrated for the first time. An improvement of 23% in reverse recovery has been obtained in experimental high voltage BJT [6]

OUTLINE OF THE THESIS

The study is divided into five chapters.

The first chapter gives an introduction to the need for faster switching power devices and the position of PIN diode and BJT amongst other competing devices. The conventional methods of improving reverse recovery are discussed followed by a description of advantages of UC with respect to these methods and the review of the work already done in this area.

In the second chapter, a theoretical framework for investigating the switching characteristics of PIN diodes is developed through modeling of effective minority carrier lifetime in the device. The dependence of effective lifetime on important device parameters and its relationship with other device specifications such as reverse blocking voltage are discussed in detail. The results obtained from the analytical model are validated and elaborated through extensive 2D numerical simulations and fabrication and characterization of diodes of different breakdown voltages. Based on this study a new improved structure for PIN diode is suggested.

In chapter three, the model developed for PIN diode is extended to discuss the switching characteristics of BJTs and the impact of insertion of universal contact within the extrinsic base region The relationship between effective minority carrier lifetime in the transistor and parameters such as collector current density and breakdown voltage are discussed in detail. The effect of universal contact on the ON state voltage $V_{CE(sat)}$ of the transistor is analyzed in detail. The results from the analytical model are validated and elaborated using 2D numerical simulations of the device and fabrication and characterization of low and high voltage transistors.

In chapter four, the process flow developed for the fabrication of low and high voltage diodes and transistors and the incorporation of universal contact within device is described in detail.

In chapter five, the important results obtained in the thesis are summarized and further extensions of the work are discussed.

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α_R	Common base current gain in reverse active mode
β_R	Common emitter current gain in reverse active mode
β_F	Common emitter current gain in forward active mode
A_{BC}	Base-collector area of transistor S-I, S-II and S-III
A_{N^+}	Area of the n^+ region of the universal contact
A_E	Emitter area
A_{LLD}	Area of low loss diode (LLD)
D_n	Average diffusion coefficient for electron
D_a	Ambipolar diffusion coefficient
E_C	Critical Electric Field for avalanche breakdown
f_L	Safety factor for left diffused region to avoid reach-through breakdown
f_R	Safety factor for right diffused region to avoid reach-through breakdown
f_B	Safety factor for base diffused region in transistor to avoid reach-through breakdown
J	Total diode current density
J_B	Base current density
J_C	Collector current density
J_E	Emitter current density
J_{hC}	Minority hole recombination current density in collector in ON state
J_{hBx}	Hole recombination current density in the extrinsic base region in ON state

J_{hC}^{S-III} Minority hole recombination current density in collector in ON state in transistor S-III

J_{hBx}^{S-III} Hole recombination current density in the extrinsic base region in ON state in transistor S-III

I Total diode current

I_L Current into the left p^+ diffused region

I_M Recombination current in the middle region

I_R Current into the right n^+ region

I_B Base terminal current

I_C Collector terminal current

I_E Emitter terminal current

I_{hC} Minority hole recombination current in collector in ON state

I_{hB} Hole recombination current in base region

I_{hBx} Hole recombination current in the extrinsic base region in ON state

I_{hBi} Hole recombination current in the intrinsic base region in ON state

k Boltzmann's constant

γ_C Injection efficiency of collector-base junction

n Ideality factor for total current

n_i Intrinsic concentration

$N_{a(x)}$ Acceptor diffused profile

N_D Collector doping

N Doping concentration

η_B Ideality factor as defined in the text

η_C	Ideality factor as defined in the text
η_L	Ideality factor for current in left diffused region current
η_R	Ideality factor for current in right diffused region
p(0)	hole concentration at collector-base junction
q	Electron charge
Q	Total charge stored in the diode/transistor
Q_L	Minority charge stored in left p^+ diffused region
Q_M	minority charge stored in middle υ region
Q_R	minority charge stored in right n^+ region
Q_p	Charge in p region (as defined in text)
Q_{hC}	Minority holes stored in collector region during ON state.
Q_{hE}	Minority holes stored in Emitter region during ON state.
Q_{eB}	Minority electrons stored in the base region during ON state
R_C	Collector ohmic resistance
R_E	Emitter ohmic resistance
ε_s	Permitivity of silicon
τ_0	Lifetime in the collector region
τ_{hB}	Time constant related to base region
τ_{hBi}	Time constant related to intrinsic base region
τ_{hBx}	Time constant related to extrinsic base region
τ_{hBx}^{S-II}	Time constant for transistor S-II
τ_{hBx}^{S-III}	Time constant for transistor S-III

τ_{eff} Effective lifetime

τ_M High-level lifetime in middle region

τ_L Time constant in left diffused region of diode

τ_R Lifetime in right diffused region of diode

T 300^0 C

V_A Applied bias

V_L Built-in voltage at the pυ junction on left side

V_{BC} Base-collector voltage in saturation

$V_{CE(sat)}$ Collector-emitter voltage in ON state

$V_{CE(sat)}^{intrinsic}$ Intrinsic collector-emitter voltage

V_{BC1} Voltage drop at x_{J2} in saturation

V_{BC2} Voltage drop in the collector region in saturation

V_{BC3} Voltage drop at x_{J3} in saturation

V_U Voltage drop in the un-modulated collector region in quasi-saturation

W_M Width of the middle υ region in diode/ conductivity modulated region in transistor

W_C Width of the collector region

x_1 & x_2 Edges of depletion layer in p diffused region

x_{J1}, x_{J2}, x_{J3} Metallurgical junction of n^+p, pυ and $υn^+$ junction

ξ_L is the fraction of the area in which n^+ has been introduced in left p^+ diffused region.

ξ_R is the fraction of the area in which p^+ has been introduced in right n^+ diffused region.

ς Fraction of extrinsic base area occupied by n^+ part of the universal contact

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CHAPTER I
INTRODUCTION

High performance semiconductor devices with better voltage and current handling capability are required in different fields like power electronics, computer and automation. Since the invention of the germanium point contact transistor in 1948[1], there has been all round progress in the science and technology of these devices. A number of new devices have been developed and old technologies have been optimized and modified by introducing better materials, designs and processes to meet the growing need for better characteristics. Besides, higher voltage and current ratings, higher switching frequency is also required for the compact design of Switch Mode Power Supplies (SMPS), for high power efficiency in variable speed motors and for better picture quality in TV deflection circuits. The power diode and transistor have been in use in such applications for a long time. The technology of these devices is quite mature. To meet the demand of still higher switching frequency, these devices are facing some inherent constraints. While operating these devices in the ON state, there is storage of minority charge carriers in various parts of the diode and transistor. These minority charges cause storage time delay and affect the voltage and current conduction processes during reverse recovery, (τ_{rr}). The dissipation in the ON state and during reverse recovery (τ_{rr}), constrain the operation of the diode and BJTs to a switching frequency of about 100 kHz. Large efforts have been made to decrease the losses in the ON state and during reverse recovery to improve the switching performance of these devices. In the

present work, we study the effect of incorporation of "universal contact" (UC) [2] on the storage of minority carriers, reverse recovery process and other characteristics of diodes and transistors. Before focusing our attention on this important topic, the present state of art of the semiconductor devices with a particular emphasis on the diode and bipolar junction transistor (BJT) is presented.

1.1 STATE OF THE ART OF TWO TERMINAL DEVICES USED FOR SWITCHING

In power circuits, active devices may be classified into two categories i.e. the two terminal devices mostly for rectification and three terminal devices as control switch. In two terminal devices we may include PIN diode and Schottky diodes. Both have their own merits. The Schottky is a low ON state voltage uni-polar device. There is no minority charge storage and hence its switching speed is fast. However, silicon Schottky diodes are limited to less than 100 volts reverse blocking voltage because of higher reverse leakage and soft breakdown. The Schottky diodes made of other material like GaAs and SiC have high switching speeds, high operating voltage and wider temperature rating [3]. But, their technology is comparatively new and materials are costlier in comparison to silicon. In medium (500-2000) and high voltage (>2000 V) operation, silicon PIN diode is the only reliable and widely used device at present. However, it has a relatively high ON state voltage and large reverse recovery time. Both of these are responsible for larger heat dissipation. To tackle the issue of higher ON state voltage and larger reverse recovery of silicon PIN diodes, three modification of the basic PIN diode structure are suggested in literature. The first is the incorporation of "universal contact"

(UC) [2], which is the focus of the present study. The second is the junction barrier controlled schottky (JBS) [4] rectifier, which is a Schottky rectifier structure with a P-N junction grid integrated into the drift region. It has low ON state voltage and smaller reverse recovery. The experimental device capable of supporting 30 volts has been demonstrated. The third device is the merged PIN/Schottky (MPS) rectifier [5] to reduce the switching losses in high voltage power rectifiers without increasing the ON state voltage. A comparison of PIN and MPS rectifiers with IGBT has been carried out for variable speed motor drives. It is shown that the switching performance of the variable motor drive improves with MPS rectifier [6] with respect to PIN diode. Thus, there has been progress in the technology of the two terminal devices and the shortcomings of the basic PIN diode are slowly being removed.

1.2 STATE OF THE ART OF THREE TERMINAL DEVICES USED FOR SWITCHING

There has been steady progress in the technology of the three terminal power devices. While consistent efforts have been made to improve the old devices like Thyristor and BJT by introducing modifications and innovations, a few new device like power MOSFET, MCT and IGBT have been developed. The extensive progress in the design and technology has resulted in the development of thyristors with a rating of 4000-8000V and 3000A. A whole variety of devices like triac, reverse-conducting thyristor, GTO (gate turn-off thyristor) and light triggered thyristor have been also developed. For the thyristor used for phase control at line frequencies the turn-off time is normally in the

range from one hundred to several hundred microseconds. When thyristors are designed and manufactured specifically to have short turn-off times, their turn-off time is several microseconds up to 50 μs [7]. In medium voltage (<1500V), BJT, MOSFET and IGBT are the desired devices. The BJT has been in use for more than 50 years. It is simple, easy to manufacture and easy to use. Millions of discrete bipolar transistors are manufactured every year. Continuous efforts have been made to understand the physics and to improve its characteristics by introducing new designs and innovations. Different models [8, 9, and 10] have been developed to enhance our understanding of this device and now are part of most simulation programs. Thousands of papers and application notes have appeared in literature dealing with all these aspects. In contrast to its low voltage counterpart, the high voltage BJT has two major limitations. One is the low gain (~10-20) and other is the large reverse recovery (1-20 μs) delay. The low gain requires large base drive and the large reverse recovery limits its operation at high switching frequency.

To overcome the problem of large base drive, larger reverse recovery delays and other constraints like current crowding etc. of BJT, two different kinds of developments have taken place. First, those who had the faith in the simplicity and ruggedness of BJT have tried to remove the shortcomings of the BJT structure and improve its characteristics. Some technological developments have taken place to improve the basic BJT structure. The doping profile of base, emitter and collector has been optimized to increase the current gain so as to reduce the base-drive, eliminate reach-through breakdown and increase the safe operating area. Connecting two BJT in monolithic Darlington configuration has, largely solved the low current gain problem of power BJT.

New emitter structures like hollow emitter, cellular emitter structure [11] and perforated emitter have been proposed. These structures basically deal with the problems of current crowding and reverse recovery. Second, there emerged a number of new kinds of devices, which showed better characteristics and solved some of the problems faced by the users of the BJT. Out of these, power MOSFET, IGBT and MCT are the important developments. Power MOSFET is different from its low voltage counterpart. The drain is made on the bottom side of the substrate instead of the same side of the source. This increases the area for current conduction and current conduction takes place through transport of majority carriers in the drift region. No delays are observed as a result of storage or recombination of minority carriers in power MOSFETs during turn off. Their inherent switching speed is orders of magnitude faster than the bipolar transistors. The transistor is controlled by voltage on gate electrode. No separate high current drive is required. Power MOSFETs have other advantages like higher safe operating area. However, these advantages are offset by high ON state resistance. As there is no injection of minority carriers to modulate the conductivity of drift region, the ON state resistance of the MOSFET is high. High on-resistance of MOSFETs limits its operating forward current density to relatively low values (typically in the range of 10 A/cm^2 for a 600 V device)[12]. Another competing device, IGBT is a hybrid of MOSFET and BJT. It incorporates the physics of bipolar current conduction with a voltage control gate of MOS. The injection of minority carriers into the bipolar drift region reduces the ON state voltage. Because of this, it is capable of operation at relatively high current densities (typically 200-300 A/cm^2), even when designed to support high voltage. These devices are being used in a number of applications.

The above two-technology i.e. of Metal-Oxide-Silicon (MOS) field effect transistor and Insulated Gate Bipolar Transistor (IGBT) have emerged as real contender of BJT power technology There is no doubt that MOSFET and IGBT have better characteristics in comparison to BJT. However, as yet these have not replaced BJT either due to higher cost consideration or due to complexity of design and manufacturing difficulties. The discrete PIN diodes and BJT are still reigning the market in medium voltage and current applications. Most important thing is that these devices still enjoy the confidence of users and manufacturers. Millions of discrete p-i-n diodes and bipolar transistors are still marketed by Motorola, Philips, Siemens and other big companies. Though, the research activity has dwindled in this area in recent times because of the maturity of bipolar technology and interest in other competing devices, it is felt that there is need to improve the switching speed of the p-i-n diodes and BJT transistors.

1.3 FOCUS OF THE PRESENT WORK

There have been developments to enhance the switching performance of diodes and transistors, such as, through Au doping and through use of Schottky clamp transistor. In 1982, Amemiya [2] introduced a concept known as universal contact to improve reverse recovery performance of diodes and transistors. Amemiya et al showed that the incorporation of n^+p^+ UC in a p^+nn^+ diode at the n^+ end resulted in significant improvement in reverse recovery and decrease in the forward ON voltage. In addition, the application of UC had an advantage when compared to the technique of Au doping to

control the reverse recovery, that it did not lead to increase of leakage current or a soft breakdown.

The incorporation of universal contact in the n^+ region such that it adjoins the lightly doped n region, works well with diodes of low or moderate breakdown voltage, but degrades the reverse blocking capability of high voltage diodes due to the onset of reach-through. Kitagawa [13] proposed the incorporation of p^+n^+ universal contact inside the diffused region of the p^+nn^+ diode away from the lightly doped region; this avoided the reach-through and still improved the reverse recovery time. Besides diodes, the universal contact has also been applied to low voltage BJTs to obtain significant reduction in storage time, Narain [14].

In the work [2,13,14], although the usefulness of the universal contact has been demonstrated, its application however has been in a limited range of current, voltage and devices. It will be further desirable to explore the effects of incorporation of UC over a wider range of current and voltage in diodes and transistors and other devices. The application of UC in a diode or transistor involves creating new diffused regions in an otherwise conventional device. The presence of these new regions alters the distribution of minority carriers and the currents flowing within the device. It is necessary to have a suitable analysis and model, which can account for the various phenomena, taking place inside the device and their influence on various parameters of the device.

1.4 OBJECTIVE OF THE PRESENT WORK

Keeping in view of the above considerations, we define the following objectives of the thesis: -

(1) To study the reduction in reverse recovery due to incorporation of universal contact and its effects on other device characteristics using a combination of analytical modeling, numerical simulation, fabrication and characterization of low and high voltage PIN diodes with and without incorporating of universal contact.

(2) To suggest changes in the design of PIN diode to achieve better characteristics.

(3) To study and model the reduction in reverse recovery due to incorporation of UC and its effects on other device characteristics using a combination of analytical modeling, numerical simulation, fabrication and characterization of low and high voltage BJT with and without incorporating universal contact.

(4) To suggest changes in design of BJT to achieve better characteristics.

1.5 OUTLINE OF THE THESIS

The study is divided into five chapters.

The first chapter gives an introduction to the need for faster switching power devices and the position of PIN diode and BJT amongst other competing devices. The conventional methods of improving reverse recovery are discussed followed by a description of advantages of UC with respect to these methods and the review of the work already done in this area.

In the second chapter, a theoretical framework for investigating the switching characteristics of PIN diodes is developed through modeling of effective minority carrier lifetime in the device. The dependence of effective lifetime on important device parameters and its relationship with other device specifications such as reverse blocking voltage are discussed in detail. The results obtained from the analytical model are validated and elaborated through extensive 2D numerical simulation [15] and fabrication and characterization of diodes of different breakdown voltages. Based on this study a new improved structure for PIN diode is suggested.

In chapter three, the model developed for PIN diode is extended to discuss the switching characteristics of BJTs and the impact of insertion of universal contact within the extrinsic base region. The relationship between effective minority carrier lifetime in the transistor and parameters such as collector current density and breakdown voltage are discussed in detail. The effect of universal contact on the ON state voltage $V_{CE(sat)}$ of the transistor is analyzed in detail. The results from the analytical model are validated and elaborated using 2D numerical simulations of the device and fabrication and characterization of low and high voltage transistors.

In chapter four, the process flow developed for the fabrication of low and high voltage diodes and transistors and the incorporation of universal contact within them is described in detail.

In chapter five, the important results obtained in the thesis are summarized and further extensions of the work are discussed.

CHAPTER II

DIODES

2.1 INTRODUCTION

The forward ON voltage, reverse blocking voltage and reverse recovery time are three important characteristics of a diode. The forward ON state voltage is required to be the lowest possible for low power dissipation, breakdown voltage the highest possible depending upon targeted application and reverse recovery time should be the least possible for faster switching. While improving the reverse recovery of the diode by the incorporation of "universal contact" (UC) no deleterious effects on the ON state voltage and breakdown voltage are desired. Keeping this in view, a brief review of these characteristics and their dependence on diode parameters is taken up before going to analysis and modeling of the effects caused by the incorporation of the UC.

The ON state voltage is comprised of built-in voltages at both diffused junctions and voltage drop in middle region. The ON state characteristics [16] of an ideal diode can be described by the relationship

$$J = \frac{4qD_a n_i}{W_M} F\left(\frac{W_M}{2L_a}\right) e^{\left(\frac{qV_A}{kT}\right)} \qquad (2.1)$$

Where V_A is the applied voltage, W_M is the width of the drift region, L_a is the ambipolar diffusion length and $F\left(\frac{W_M}{2L_a}\right)$ is a function given as under

$$F\left(\frac{W_M}{2L_a}\right)=\frac{\left[\left(\frac{W_M}{2L_a}\right)\tanh\left(\frac{W_M}{2L_a}\right)\right]}{\sqrt{1-\frac{1}{4}\tanh^4\left(\frac{W_M}{2L_a}\right)}}e^{-\left(\frac{qV_M}{2kT}\right)} \qquad 2.1(a)$$

Where V_M, is the voltage drop in the middle region. As seen from Fig. 2.1, the function $F\left(\frac{W_M}{2L_a}\right)$ is maximum when half of the drift region width $(\frac{W_M}{2})$ is equal to the diffusion length, L_a. Thus, as the speed of the rectifiers is increased through the lifetime reduction while keeping the W_M constant, it would be accompanied by deterioration in

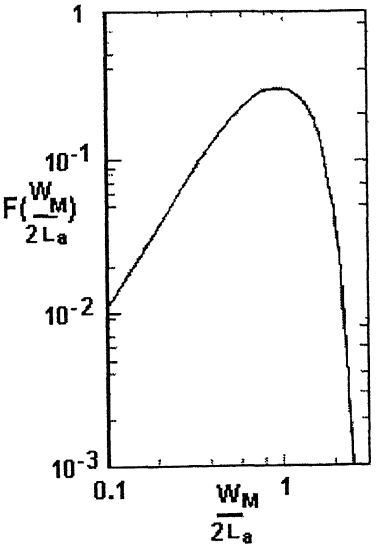


Fig. 2.1 Function F ($W_M/2L_a$)

the forward ON voltage if initially the design is optimal ($W_M = 2\ L_a$). This illustrates an important trade off that exists between the switching speed and the forward voltage drop in the design of the power diode. The current and related voltage drops have been extensively studied [17-20].

The doping and the width, W_M of the drift region determines the breakdown voltage of the diode. For better forward characteristics, lower W_M is desirable as seen from Eq. (2.1). As the forward current density is independent of the background doping, the width is optimized to be minimum by lowering the background doping for a given breakdown voltage. The power diodes are usually made of punch-through type i.e. their width; W_M is less than the depletion width at the avalanche breakdown. The punch through voltage, V_{PT} for a parallel plane junction is given by

$$V_{PT} = E_C W_M - \frac{q N_D W_M^2}{2\varepsilon_s} \qquad (2.2)$$

The critical electric field is a weak but increasing function of doping [21] and increases with increase in doping. Taking this variation in the critical electric field into consideration, an optimum width and doping can be found out for parallel plane junction.

The junctions are usually made by diffusion using oxide masks. This process results in spherical and cylindrical junctions at corners and edges respectively. Due to this reason, the actual breakdown voltage in planar junctions is about 50% of the parallel plane junction. At high voltage the curved junction give rise to high fields near the surface and this induces ionic instability at the surface which causes increased leakage

and soft breakdown. As a result, the curved portions are chemically etched out and passivated in high (>500 V) voltage devices. One of the methods to remove curved portion is the mesa etching. The etched portion is then filled with glass to passivate the junction. The actual breakdown voltage is restored to 80% of the parallel plane junction. The effect of edge termination technique upon the breakdown voltage and its relationship with the width and doping of the drift region has been summarized in Table 'A'. In high voltage diodes the doping of the drift region is low and width is large. Due to the low doping of the drift region, lifetime in the diode is high and this degrades the reverse recovery.

The reverse recovery time depends on the total charge stored in the diode in the ON state. A high lifetime in the middle drift region leads to large minority charge storage in the diode. Further, the structure of the conventional diode keeps the minority charge confined to the large drift region. Generally, the diode has a p^+-υ-n^+ type of structure as shown in Fig. 2.2(a). In high voltage diodes, p^+ and n^+ are diffused in a bulk wafer. Low voltage diodes are typically made by p^+ diffusion in n on n^+ epitaxial wafer. The diffused regions give rise to electric fields due to the concentration gradient [22]:

$$E = \frac{kT}{q}\frac{1}{N}\frac{dN}{dx} \qquad (2.3)$$

This electric field is also evident in the band diagram shown in Fig. 2.2(b). In the ON state, the electric field opposes the transport of minority carriers across the diffused regions. The injected electrons in left p-diffused region face opposing electric field due to this concentration gradient and similarly, the holes also face opposing electric field in the

right n-diffused region. In case of n-n^+ epitaxial interface, the dN/dx gradient is very sharp and opposition to minority carriers greater and consequently there is little penetration of minority carriers across this layer. This results in the minority charge being confined to the middle drift region. When the device is turned off, the current continues to flow in the device till all the minority charge is removed. This effect gives rise to long reverse recovery which consists of constant reverse current phase called storage time and 90% of the fall time delay.

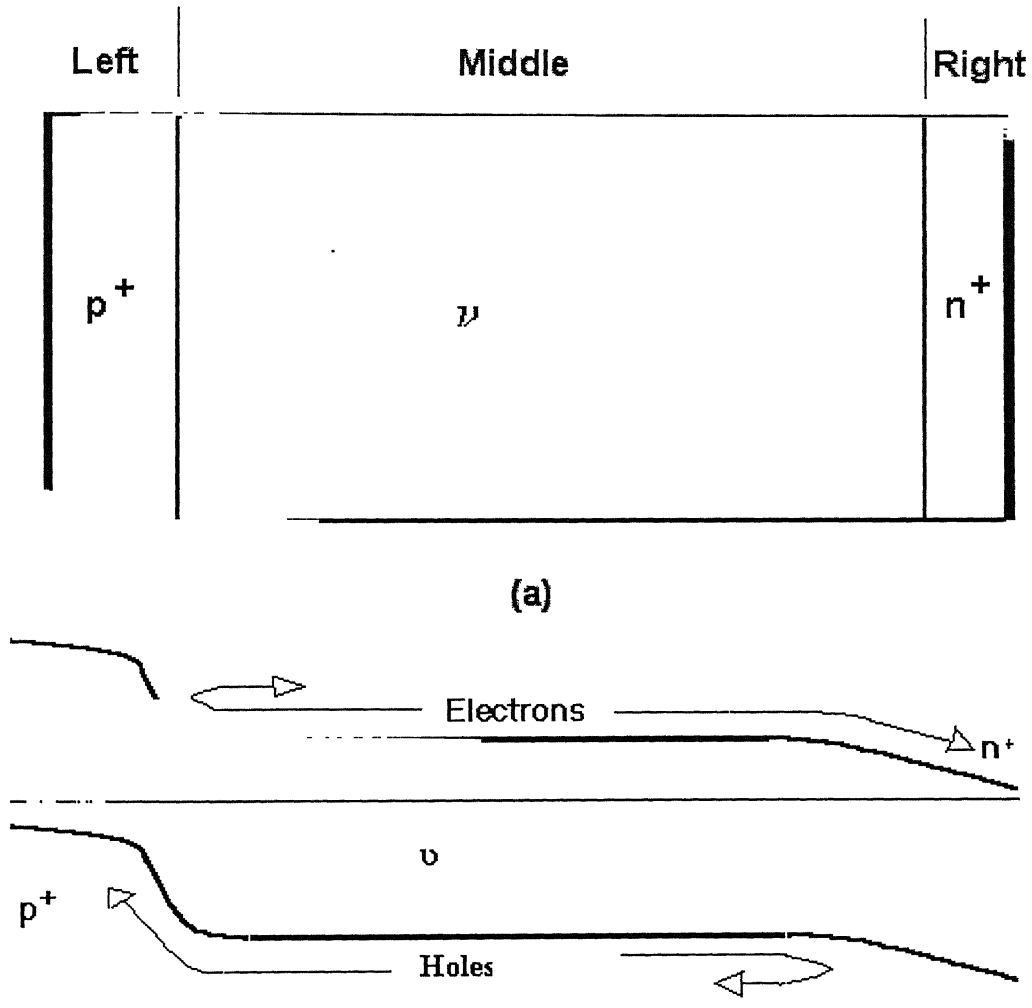


Fig. 2.2 **(a) Conventional diode structure (S-I) and its (b) Band diagram with carrier flow directions**

2.2 DIODE STRUCTURE (S-II) TO REDUCE THE REVERSE RECOVERY AND TO DECREASE 'ON' STATE VOLTAGE

In conventional diode structures shown in Fig. 2.2(a) most of the minority charge is stored in the lightly doped υ region. The holes that are injected into this region are confined by the reflecting υn$^+$ contact as explained earlier. In the device proposed by Amemiya [2] et al shown in Fig. 2.3, henceforth referred to as structure S-II, an additional path for exit of holes from the lightly doped region has been provided through incorporation of the p$^+$ diffusion in a mosaic pattern alternate with n$^+$ diffusion. The n$^+$p$^+$ when connected with a common metal form an equi-potential contact, called "universal contact" (UC) as it is truly ohmic for both electrons and holes. It has been shown [2] that the introduction of universal contact leads to significant reduction in reverse recovery time and also lowering of the 'ON' state voltage.

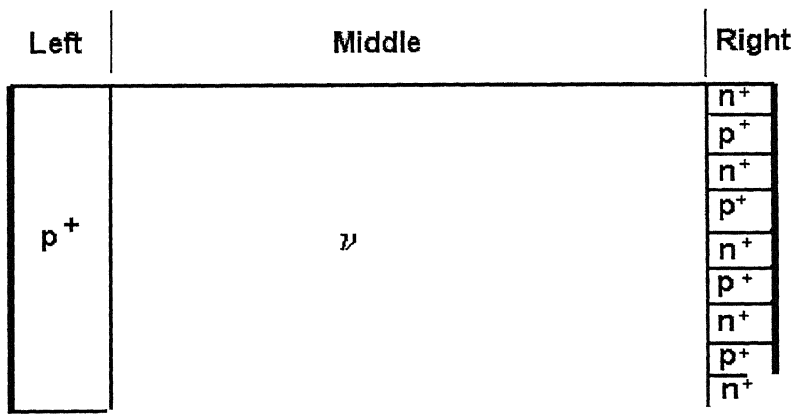


Fig. 2.3 Diode incorporating "universal contact" (S-II)

Though, there is significant improvement in reverse recovery by incorporating the universal contact as done in Amemiya structure Fig. 2.3, this approach cannot be applied to conventional high voltage diode structures due to the following reasons.

1. To isolate the devices, grooves have to be formed around the edge of each device extending to interface between the v-type epitaxial layer and the p+ substrate to create individual diode [23]. This can easily be done for thin epiaxial layer. For high voltage diode made in epitaxial wafers of 50 – 100 μm epi-layer or in bulk devices, it is not convenient.

2. The diode structure as shown in Fig. 2.3 in effect becomes a $p^+\upsilon p^+$ side by side the $p^+\upsilon n^+$ due to the extension of p^+ diffused region for making the universal contact up to the edge of the nn^+ interface. In low voltage diodes, the doping of the drift region is comparatively high. On application of reverse bias, depletion layer starting from the $p^+\upsilon$ junction do not extend to the back p^+n^+ universal contact before the reverse avalanche breakdown takes place. In high voltage diodes though the drift region width is large, the depletion layer quickly extend to other end on application of high reverse bias due to the inverse quadratic depends of depletion layer on drift region doping. As seen from the Table 'A', the doping of the drift region of high voltage diode is approximately two orders of magnitude smaller in comparison to low voltage diodes. This results in the extension of the depletion layer to the edge of p^+n^+ universal

contact, which causes reach through reverse breakdown. This reach through breakdown is different from the reverse breakdown in the $p^+\upsilon n^+$ punch-through diodes discussed in the last section. In the punch-through diode, the phenomenon of avalanche multiplication due to the high electric field causes reverse breakdown. The reach through breakdown of $p^+\upsilon p^+$ high voltage diode structure incorporating universal contact (S-II) takes place at a much lower voltage in comparison to avalanche breakdown.

2.3 MODIFIED DIODE STRUCTURE (S-III)

To avoid the above problems, a diode structure shown in Fig. 2.4, henceforth called the diode structure S-III has been proposed by Kitagawa [13]. The important feature of the S-III is that the UC has been incorporated within the diffused region away from the junction. In reverse mode, most of the depletion layer extends into low-doped ν region. The diffused p^+ region inhibits depletion layer extending into it and thus avoids punch-through. It is shown that the reverse recovery and forward ON voltage in S-III are smaller than in S-I. As seen above, the original concept of universal contact has been suitably modified for high voltage diodes to realize a shorter reverse recovery and low ON state voltage. With the coming up of the new applications for faster switching, further understanding of the mechanisms of reduction of reverse recovery by the incorporation of UC is desirable.

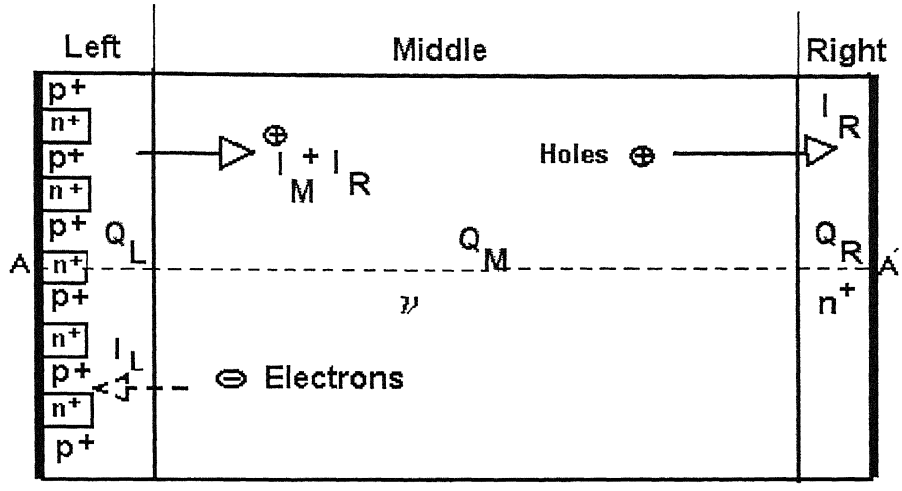


Fig. 2.4 Modified diode structure (S-III)

Keeping this in mind, efforts have been made in next sections to analyze and model the effect of charge storage, current conduction in diode and the effect of the incorporation of UC in diode on reverse recovery and other important characteristics.

2.4 MODELLING & SIMULATION OF EFFECTIVE LIFETIME

The improvement in switching delay obtained through incorporation of universal contact in S-II and S-III can be viewed from another angle, aside from the mechanism of providing another path for exit of carriers from the lightly doped region. The switching delay is closely related to the effective minority carrier lifetime in the device defined as

$$\tau_{eff} = \frac{Q}{I} \qquad (2.4)$$

Where Q is the total minority charge stored and I, is the total current flowing through the diode. Fig. 2.5 shows a comparison of the effective lifetime for a conventional diode structure, S-I along with the total reverse recovery time as a function of current density. These results were obtained through 2D numerical simulation using the Silvaco device simulation package [15] for a diode of breakdown voltage of 1000 Volts. The description of the diode is given in Table 2.1.

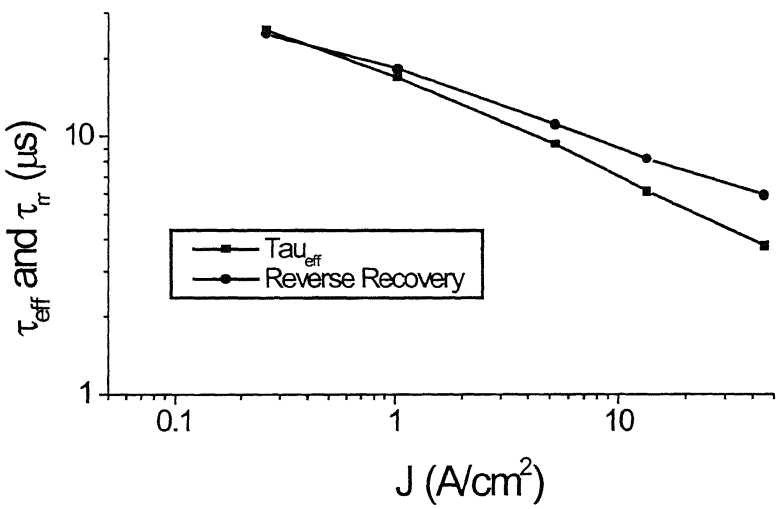


Fig. 2.5 **Comparison of reverse recovery (τ_{rr}) and effective lifetime (τ_{eff}) as a function of current density for high voltage diode (S-I)**

The 2D simulations are based on drift-diffusion formalism and take into account the concentration dependent SRH recombination, concentration and field dependent mobility, band gap narrowing and Auger effects. The reverse recovery time is defined as the total time for which the diode conducts in the reverse direction and is the sum of

storage and fall times. It can be seen from the figure that the effective minority carrier lifetime tracks total reverse recovery time quite well. Although, reverse recovery waveform can be quite complicated with several distinct regions such as storage time, fall time etc, for ease of analysis, the subsequent discussion will deal primarily with the effective lifetime.

The current I in Eq. (2.4) can be divided into three components [24], the minority electron current injected into the left region I_L, hole recombination current I_M, in the middle region and hole current I_R injected into the right region. Similarly, the minority charge Q, can be considered as having three components Q_L, Q_M and Q_R in the left, middle and right regions respectively. With these definitions, τ_{eff} may be re-written as

$$\tau_{eff} = \frac{\tau_M \bullet \left(1 + \frac{Q_L}{Q_M} + \frac{Q_R}{Q_M}\right)}{\left(1 + \frac{I_L}{I_M} + \frac{I_R}{I_M}\right)} \qquad (2.5)$$

Where $\tau_M = \frac{Q_M}{I_M}$ is high-level injection lifetime in the lightly doped middle region.

It is a fairly good assumption that the minority charges Q_L, Q_R in the p and n-regions are much smaller than the minority charge Q_M in the middle region because the doping in left and right regions are much larger as compared to that in the middle region.

However, the currents injected into the left and right regions are not negligible so that the Eq. (2.5) can be simplified to

$$\tau_{eff} = \frac{\tau_M}{\left(1+\frac{I_L}{I_M}+\frac{I_R}{I_M}\right)} \qquad (2.6)$$

Eq. (2.6) can be re-written in an alternative form as

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_L} + \frac{1}{\tau_M} + \frac{1}{\tau_R} \qquad (2.7)$$

Where $\tau_L = \tau_M I_M/I_L$ and $\tau_R = \tau_M I_M/I_R$.

Eq. (2.7) shows that the effective minority carrier lifetime in the diode is a function of three time constants and only one of which is the recombination lifetime in the lightly doped middle region. The conventional approach for improving reverse recovery, under the tacit assumption $\tau_{eff} \cong \tau_M$, have accordingly focussed attention on reducing this lifetime through incorporation of impurities such as Au, Pt etc. Eq. (2.7) however, suggests other alternative techniques for reducing the effective minority carrier lifetime by reducing other time constants such as τ_L or τ_R. The expressions for these time constants show that this would require an increase of either the I_L/I_M or the I_R/I_M current ratios. The reason for this improvement is that while a thick, lightly doped middle region is well suited for the task of reverse blocking, it is unsuitable for carrying a

substantial share of minority carrier current due to high recombination lifetime. On the other hand, the heavily doped n^+ and p^+ regions of the diodes, are better suited to carry a larger fraction of minority carrier current because of lower recombination lifetimes in these regions. Accordingly, as indicated by Eq. (2.6), it makes sense to divert minority carrier current away from the lightly doped middle region to other regions of the diode where lifetime is lower. This principle, of diverting current away from regions of high recombination lifetime to regions of low recombination lifetime is well known and applied for example in BJTs, where sometimes a Schottky diode is connected across the collector-base junction so as to improve the transistor's switching performance. In this case a large fraction of the base current in saturation is diverted from the collector-base junction of the transistor, where minority carrier lifetime is high, to Schottky diode, which is characterized by negligible minority carrier storage. The use of universal contact provides a mechanism for implementing this principle within PIN diodes as explained in detail below.

Let us consider how the ratio I_L/I_M can be increased so as to reduce the effective recombination lifetime. The current I_L results from injection of electrons into the p-diffused left region. These electrons are normally reflected back by the sharply increasing p-type doping profile, thus limiting the minority carrier current I_L to a small value. However, if a "universal contact" is incorporated in the diffused region, the minority carrier current I_L can be significantly increased. This contact should however be inserted so that, there is no reach-through prior to avalanche breakdown when the diode is in the reverse blocking state. This can be done by restricting the depth of n^+ diffusion to less than the extent of the depletion layer at the breakdown voltage. This structure is expected

to result in improvement in switching performance but without any decrease in reverse breakdown voltage.

To verify the above concept, the diodes S-I and S-III were studied through 2D numerical simulations. The details of the structure of the diodes are listed in Table 2.1. Both, the diodes are designed for a breakdown voltage of ~150 Volts.

Table 2.1 - Details of the Simulated Diodes

Diodes	Base Resistivity/ Doping and Width	n^+ substrate/ Right side N^+ diffused Region thickness and doping	p diffusion	p^+ diffusion for making "universal contact"	n^+ diffusion in p for "universal contact" (Refer Fig.2.4)
(1)Low Voltage (S-1 & S-III) (~ 150 V)	nn^+ epi, n width 15 μm & Conc.1.15 x 10^{15} /cm^3.	n^+ substrate thickness 300 μm, Doping > 10^{20}/cm^3.	Xj=5.7 μm, Surface Conc. 2 x 10^{18}	Xj=1.6 μm, Surface Con 2.0 x 10^{19}	Xj=3.0 μm, Surface Con. 4.0 x 10^{20}
(2)High Voltage (S-1 & S-III) >1000 V)	4 x 10^{13} /cm^3, 140 μm Bulk silicon,	n^+ Right side diffused region thickness 35 μm, Surface con. ~ 4x10^{18} /cm^3.	Xj=22 μm, Surface Conc. 7 x 10^{17}	Xj=2.2 μm, Surface Con 5.0 x 10^{19}	Xj=4.1 μm, Surface Con. 8 x 10^{19}

Fig. 2.6 shows a comparison of the effective lifetime obtained for the low voltage diodes S-I and S-III. The effective lifetime decreases from 849 ns to 194 ns, a reduction of 77% at 1 A/cm^2 and from 88 ns to 28 ns a reduction of 68% at about 110 A/cm^2.

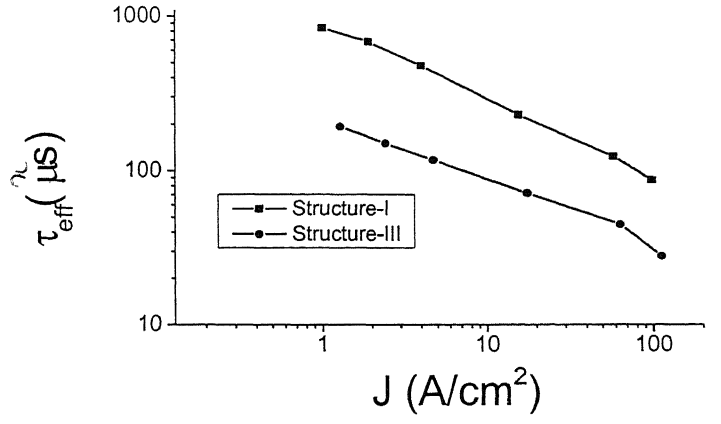


Fig. 2.6 τ_{eff} vs J for low voltage diodes (S-I & III)

The improvement in effective lifetime obtained was found to be similar to the improvement observed in reverse recovery under both hard and soft switching conditions indicating that effective minority carrier lifetime is a good and simple measure of the switching performance of the diode.

Fig. 2.7 shows a comparison of effective lifetime of the two structures designed for reverse blocking voltage of around 1000 V. In these high voltage diodes, τ_{eff} decreases from 26 μs to 15.4 μs, a reduction of 41% at 0 3 A/cm^2 and from 3.8 μs to 2.3 μs, a reduction of 39% at about 50 A/cm^2.

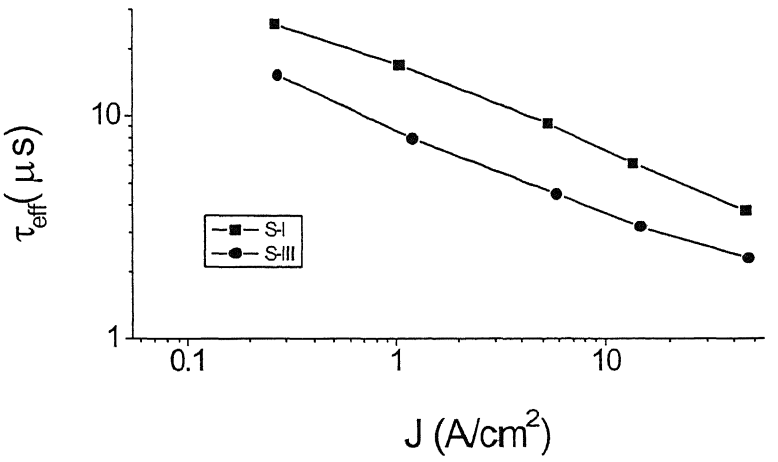


Fig. 2.7 τ_{eff} vs J for high voltage diode (S-I & III)

These results can be explained in terms of changes in the current ratio I_L/I_M. Figs. 2.8 and 2.9 show a comparison of the ratio I_L/I_M for the low and high voltage diodes respectively.

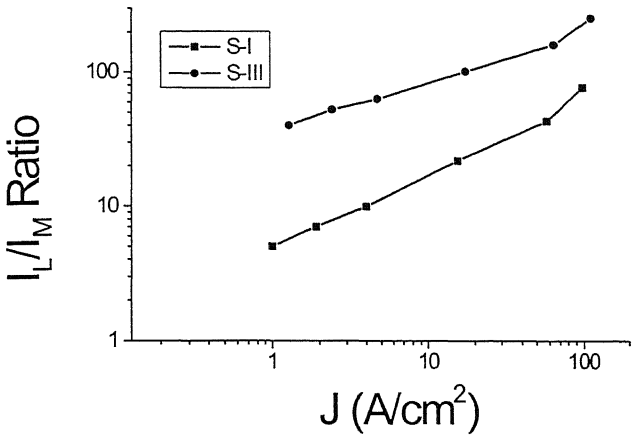


Fig. 2.8 **I_L/I_M ratio for low voltage diodes (S-I & III)**

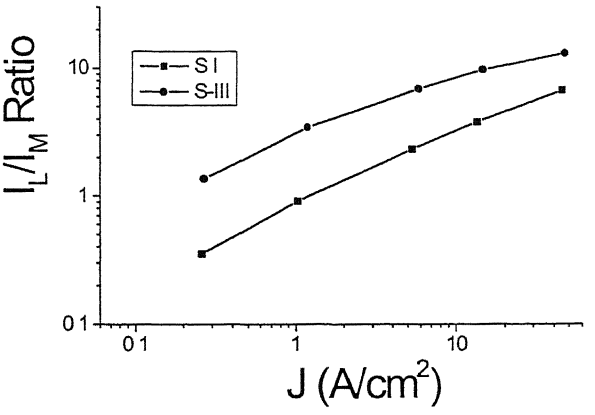
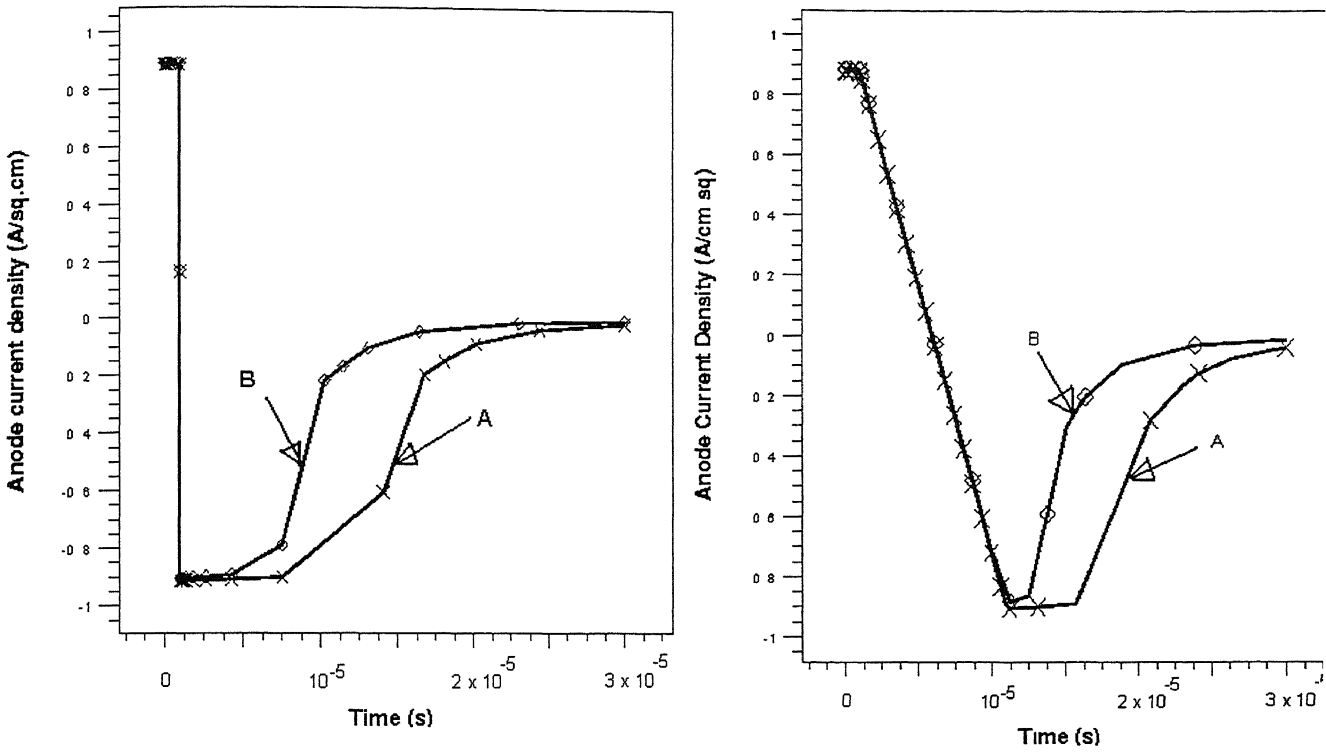


Fig. 2.9 **I_L/I_M ratio for high voltage diodes (S-I & III)**

The reduction of reverse recovery time by 77% for the low voltage case can be largely attributed to an increase of the ratio I_L/I_M, from 5 to 38.6. Similarly, the results for high voltage diode can be attributed to improvement in the I_L/I_M ratio.

Fig. 2.10 (a) and (b) shows the two representative simulated reverse recovery waveforms under hard and soft reverse recovery respectively using resistive load. The forward voltage is 4.7 V and reverse voltage is 3.5 V. In Fig. 2.10 (b), the voltage is ramped from forward voltage to reverse peak voltage in 10 μs. In step recovery; the same was done in 2 ns. The effective lifetimes as obtained either from hard or soft recovery is same.



(a) (b)

Fig. 2.10 **Simulated current waveform under (a) hard/step Recovery (b) soft/ramp Recovery**
(Waveform marked 'A' is for diode S-I and 'B' for diode S-III)

2.5 MODELING & SIMULATION OF DEPENDENCE OF END CURRENTS ON DEVICE PARAMETERS

The variation of the current ratio I_L/I_M with current density and also the difference in effective lifetime between the low and high voltage diodes can be explained using a simple analytical model. Fig. 2.11 shows a 1D view of the device in the region where n^+ diffusion in p-diffused region has been made. The x_{j1}, x_{j2} and x_{j3} are the metallurgical

junctions of front n^+p "universal contact", pυ diode and back $υn^+$ contact. The x_1 and x_2 are the depletion edges of n^+p and pυ junctions inside the p diffused region.

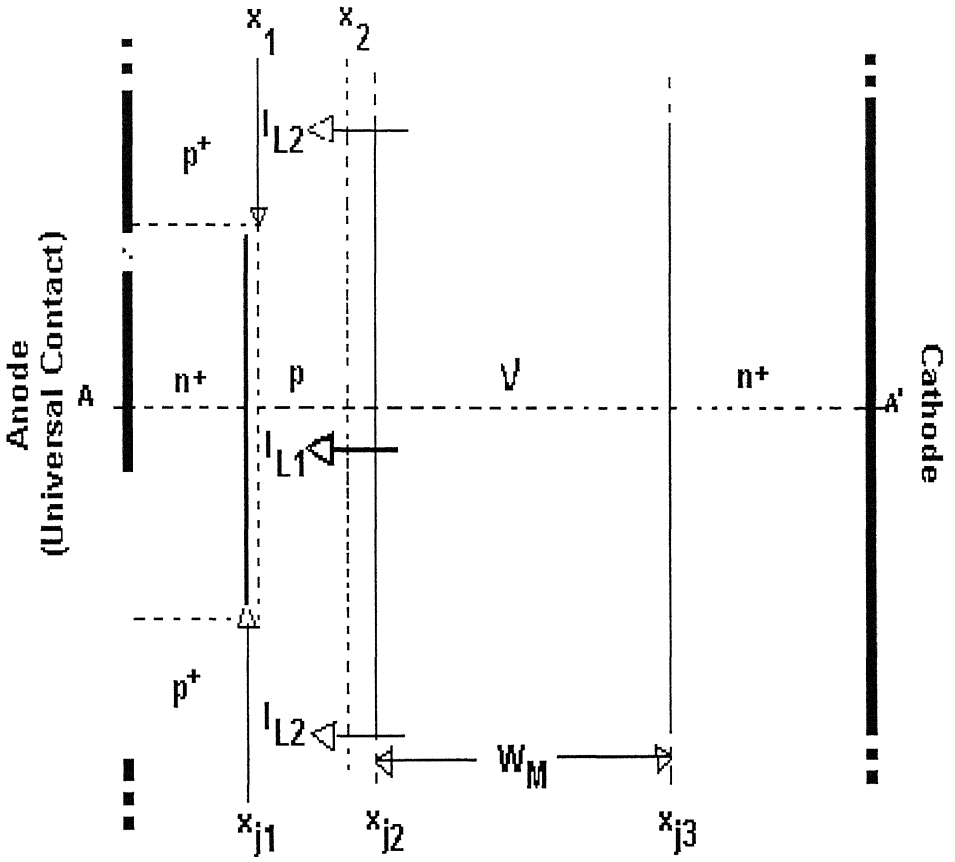


Fig. 2.11 **One dimensional diode structure under n^+ (At cross - section A-A') of Fig. 2.4**

Since the current ratio I_L/I_M is the most important factor affecting the minority carrier lifetime, let us look at some of the important factors that influence this ratio. The current injected into the left region can be divided into two components: a component, I_{L1}

flowing under n^+ and other component, I_{L2} under p^+. Since $I_{L1} >> I_{L2}$, $I_L \approx I_{L1}$. Under steady forward bias conditions, the current density I_L due to electron flow in the left p-diffused region can be written [25] as

$$I_L = \frac{q^2 n_i^2 D_n \exp\left(\frac{qV_L}{kT}\right)}{Q_p} \xi_L A \qquad (2.8)$$

Where A is the area of the diode and ξ_L is the fraction of the area in which n^+ has been introduced. Defining a factor $\eta_L = \frac{V_A}{V_L}$, where V_A is the applied voltage, equation (2.8) may be written as

$$I_L = q^2 n_i^2 D_n A \frac{\exp\left(\frac{qV_A}{\eta_L kT}\right)}{Q_p} \xi_L \qquad (2.9)$$

For simplicity, we assume that when junction is forward biased $x_2 = x_{j2}$ and low level injection conditions prevail so that $Q_p = q \int_{x_1}^{x_{j2}} N_a(x)\,dx$. To avoid reach-through prior to onset of avalanche breakdown, we require that at breakdown $(x_{j2} - x_1) > 0$. Taking E_C as the critical field, we obtain the condition

$$\frac{q}{\varepsilon_s} \int_{x_1}^{x_{j2}} N_a dx > E_C \qquad (2.10)$$
$$or\ Q_p > \varepsilon_s E_C$$

Defining $f_L = \frac{Q_p}{\varepsilon_S E_C}$, allows Eq. (2.9) to be re-written as

$$I_L = q^2 n_i^2 D_n A \frac{\exp\left(\frac{qV_A}{\eta_L kT}\right)}{f_L \varepsilon_s E_C} \xi_L \qquad (2.11)$$

The factor f_L represents a safety factor in the sense that for $f_L > 1$, the charge, Q_p under the universal contact is large enough to prevent onset of reach-through prior to onset of avalanche breakdown. On the other hand if $f_L < 1$, then the reverse blocking voltage would be determined primarily by the occurrence of reach-through.

The middle region current, I_M is the minority carrier current and can be modeled as recombination current [17], which may be written as

$$I_M = qn_i A \frac{W_m}{\tau_M} \exp\left(\frac{qV_A}{\eta_M kT}\right) \qquad (2.12)$$

Where η_M is the ideality factor of the current, I_M. The ratio I_L/I_M can now be obtained using Eq. (2.11) and Eq. (2.12) as

$$\frac{I_L}{I_M} = q\, n_i D_n \frac{\tau_M}{W_M} \frac{\exp\left(\frac{qV_A}{kT}\left(\frac{1}{\eta_L} - \frac{1}{\eta_M}\right)\right)}{f_L \varepsilon_s E_C} \xi_L \qquad (2.13)$$

The total current density J of the diode may be written in terms of its ideality factor n as

$$J = J_O \exp\left(\frac{qV_A}{nkT}\right) \qquad (2.14)$$

Equation (2.14) can be used to re-write Eq. (2.13) as

$$\frac{I_L}{I_M} = C_L \frac{\tau_M}{W_M} \frac{J^{\alpha_L}}{f_L} \xi_L \qquad (2.15)$$

Where $\alpha_L = n \times \frac{\eta_M - \eta_L}{\eta_M \eta_L}$ and constant factor, $C_L = \frac{q\, n_i\, D_n}{\varepsilon_s E_C\, J_0^{\alpha_L}}$

Substitution of Eq. (2.15) in Eq. (2.7) and neglecting the ratio I_R/I_M that is smaller than the ratio I_L/I_M, we obtain

$$\frac{1}{\tau_{eff}} \cong \frac{1}{\tau_M} + \frac{1}{\tau_L} \qquad (2.16)$$

Where $\tau_L^{-1} = C_L \frac{J^{\alpha_L}}{f_L W_M} \xi_L$

Equation (2.16) predicts that the effective lifetime will decrease with increase in current density. This is due to the different ideality factors of the current injected into the middle and the left regions of the diode. A plot of the ideality factors for three different current components as extracted from simulations using Eq. (2.17) of diode S-I is shown in Fig. 2.12.

$$\eta = \frac{q}{kT} \Delta V \ln\left(\frac{J_2}{J_1}\right) \qquad (2.17)$$

ΔV is the change in applied voltage when the current density is varied from J_1 to J_2. The value of η_M is ~2 and that of η_L and η_R is ~1.

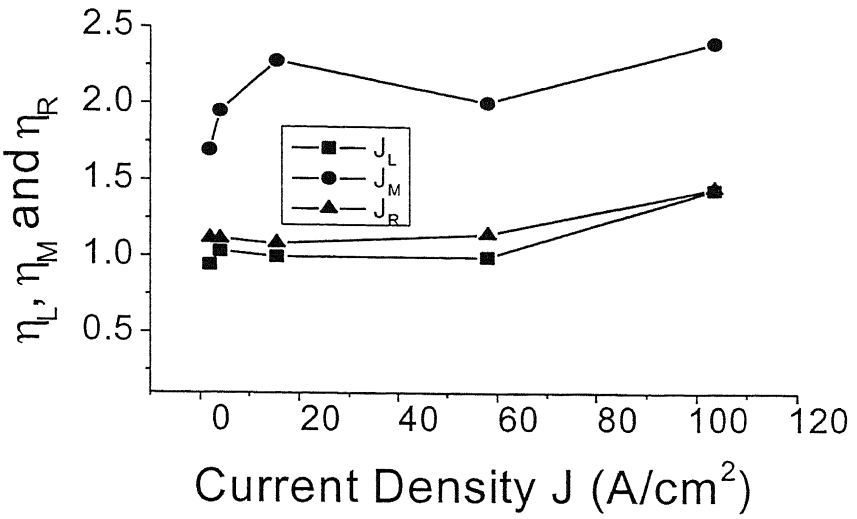


Fig. 2.12 - J vs Ideality Factor for end region currents and middle region current for low voltage diode (S-I)

The minority hole current in the middle region increases as $\exp\left(\frac{qV_A}{2kT}\right)$ due to high level injection in the middle region, while the current injected into the left region increases as $\exp\left(\frac{qV_A}{kT}\right)$ due to low level injection condition, causing the ratio I_L/I_M to increase with increase in bias or the time constant τ_L to decrease with increase in current density.

Eq. (2.16) also shows that the impact of insertion of universal contact on effective lifetime will decrease as the breakdown voltage of the diode increases. This is because; increase of breakdown voltage requires increase of the thickness W_M of the lightly doped middle region, which increases the time constant τ_L. Thus, like the conventional PIN

diode, in this case also, there is a tradeoff between the reverse recovery and the reverse blocking voltage.

Instead of the left p^+ region, the universal contact can also be inserted in the right n^+ region. For this case, an expression similar to Eq. (2.16) can be written

$$\frac{1}{\tau_{eff}} \cong \frac{1}{\tau_M} + \frac{1}{\tau_R} \tag{2.18}$$

Where $\tau_R^{-1} = C_R \frac{J^{\alpha_R}}{f_R W_M} \xi_R$

Both Eq. (2.16) as well as Eq. (2.18) shows that a decrease in safety factors can result in improvement in the effective lifetime. In fact, f_R may be made even less than unity by inserting the universal contact deeper into the n^+ region. In this case the reverse blocking voltage would be compromised due to onset of reach-through prior to avalanche breakdown. This illustrates that the reverse blocking characteristics can be traded with the switching characteristics in a new manner determined by the proximity of the universal contact to the edge of the lightly doped region. This is exactly what is done in the structure S-II proposed by Amemiya et al, where the universal contact is inserted in the right n^+-region of the diode such that it is contiguous with the middle region. Although Eq. (2.18) ceases to hold when f_R becomes zero, we expect that a large decrease in effective lifetime would result at the expense of a drop in the reverse blocking voltage especially in diodes designed for high voltage operation. This is illustrated in Fig.

2.13 where the structures S-I and S-II are compared. As can be seen, the effective lifetime is significantly reduced in diode S-II in comparison to conventional diode S-I.

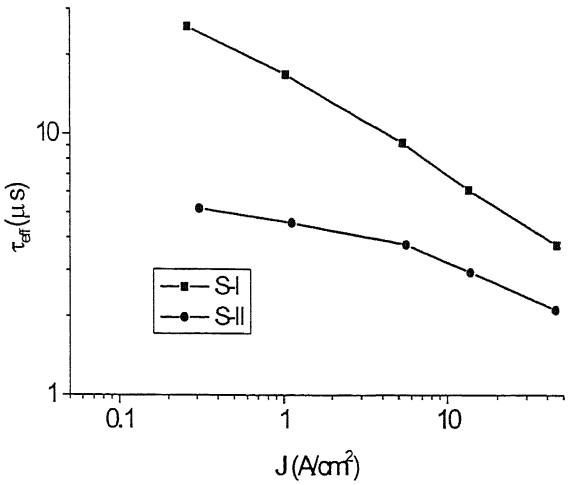


Fig. 2.13 τ_{eff} vs J of high voltage diode (S-I and S-II)

Fig. 2.14 shows a comparison of the ratio I_R /I_M for the two structures, S-I and S-II. The increase in this current ratio for S-II completely accounts for its better performance.

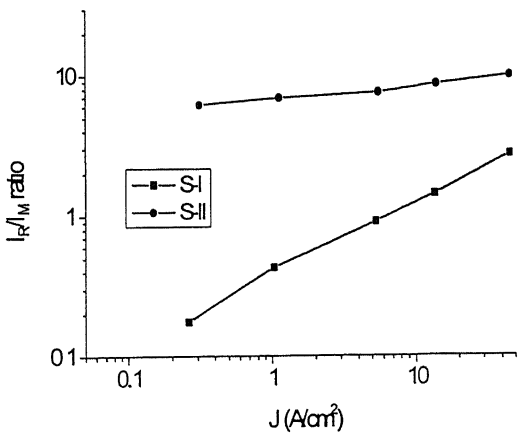


Fig. 2.14 I_R/I_M for high voltage diode (S-I & II)

The simulated reverse characteristics of diode S-I and S-II are shown in Fig. 2.15. It can be seen that the diode S-II suffers from premature breakdown due to reach-through between the two p^+ regions, one on the left and the other on the right side

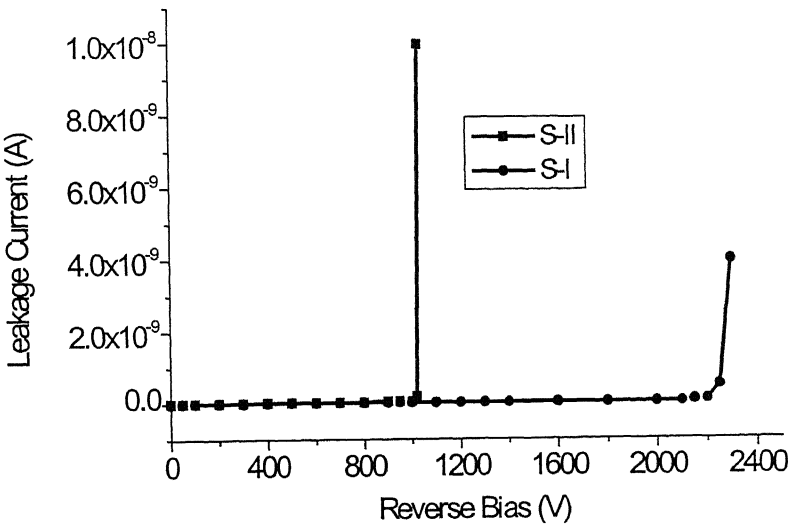


Fig. 2.15 Simulated breakdown voltage of diodes (S-I & II)

The onset of this p^+-n-p^+ reach-through in S-II limits the reverse blocking voltage to less than half the breakdown voltage of the conventional diode S-1. This reach-through phenomenon is either absent or less severe in low voltage diodes because the doping in the middle region is relatively high and as a result, the depletion layer on application of reverse bias does not reach the p^+ region even at breakdown voltage.

During reverse recovery, the reverse current consisting of holes flows only through the p^+ part of the universal contact. This results in lateral current flow and voltage drop under the n^+ regions of the universal contact as illustrated in Fig. 2.16, which may result in turn-on of the parasitic n^+pvn^+ transistor [26]. To determine whether this is likely to happen or not, let us try to estimate the lateral voltage drop at current densities of interest. Taking the approximation that the current flows in lateral x direction under n^+, this may be analyzed by taking a single n^+ diffusion of width, L inside p^+ region as shown in Fig. 2.16.

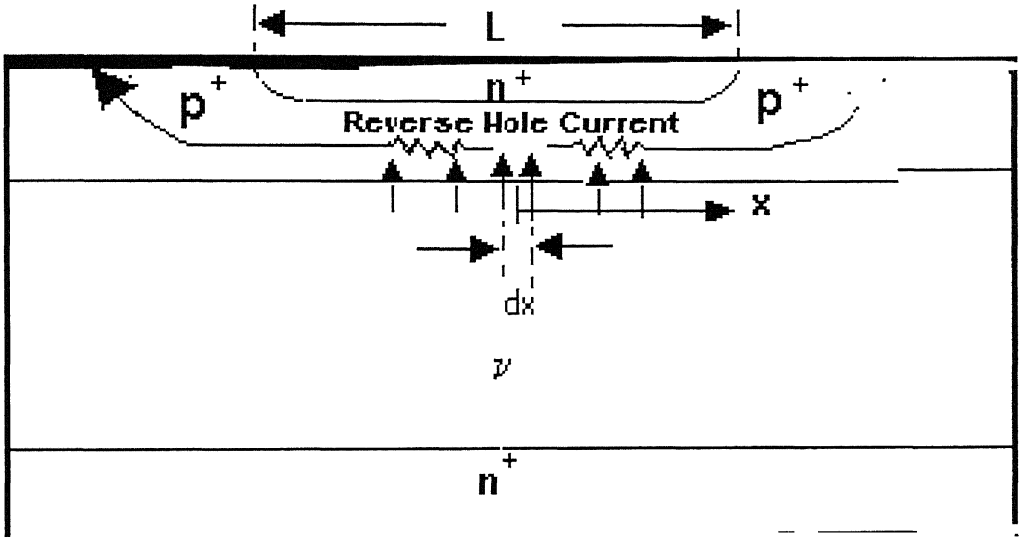


Fig. 2.16 Universal contact region showing flow of current under n^+ in reverse bias condition

Taking $x = 0$ at the center of n^+ finger, the current under n^+ may be written as

$$I(x) = \int_0^x J_z \, dx = J_z x \qquad (2.19)$$

Where z is the dimension perpendicular to the plane of the paper.

$$dV(x) = I(x) \quad \frac{\rho_S}{z} dx \qquad (2.20)$$

Where ρ_S is the sheet resistance of the diffused region and dV is the small voltage drop across small distance dx.

$$V = \int_0^{L/2} dV_{(x)} dx = J \rho_S \int_0^{L/2} x\, dx \qquad (2.21)$$

$$= J \rho_S \frac{L^2}{4}$$

Assuming that V = 0.7 V is required to turn on the parasitic NPN transistor, the width of the n^+ contact for which the parasitic transistor may turn ON has been calculated as a function of current density and is given for few current density values.

For 100 A/cm^2, L= 167 μm;

For 500 A/cm^2, L= 74.8 μm;

For 1000 A/cm^2, L= 52.9 μm;

ρ_S = 100 Ω/sq. has been assumed.

These results indicate that for a width of 60 μm, there is no possibility of turn-on of the parasitic transistor. These results were confirmed through simulation and it was found through that for $n^+ : p^+$:: 60 μm : 40 μm, the voltage difference under p^+ and n^+ is

only a few mV and turn-on of the parasitic transistor has not been observed even under hard reverse recovery.

2.6 A Proposed Diode Structure

The improvement in effective minority carrier lifetime would be maximum when "universal contact" is incorporated in both the left p^+ and the right n^+ regions as illustrated in Fig. 2.17, henceforth referred to as diode S-IV. By keeping the safety factors larger than unity, the new structure is expected to give significant improvement in effective lifetime without compromising the reverse blocking voltage.

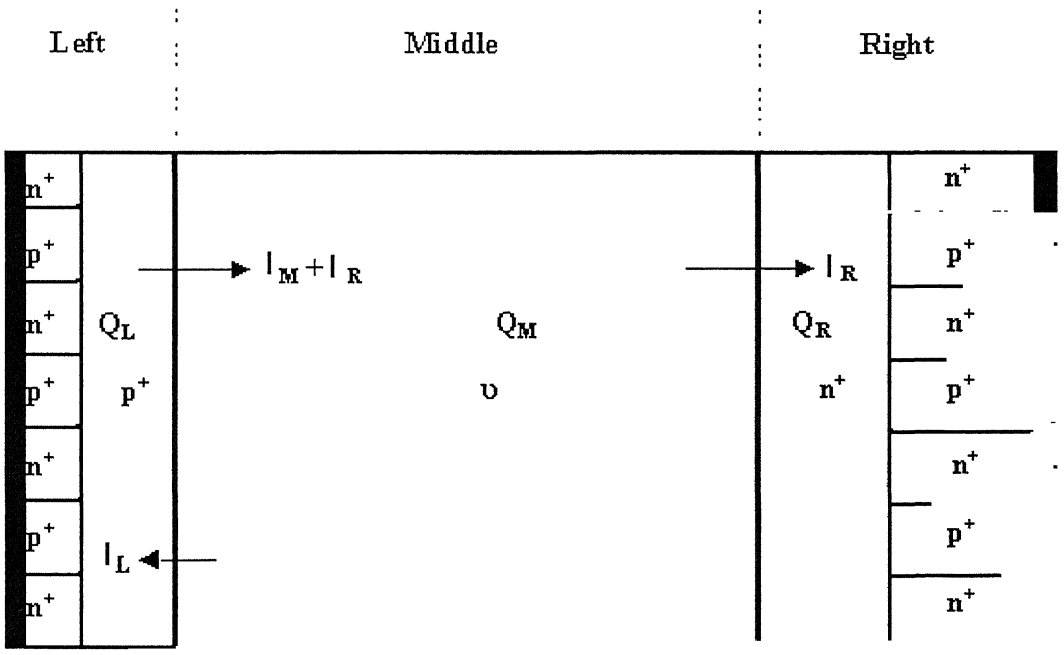


Fig. 2.17 A proposed diode structure (S-IV)

A comparison of effective lifetimes for the structures S-I, II, III and IV is shown in Fig. 2.18 for a diode designed for reverse blocking voltage of >1000 Volts.

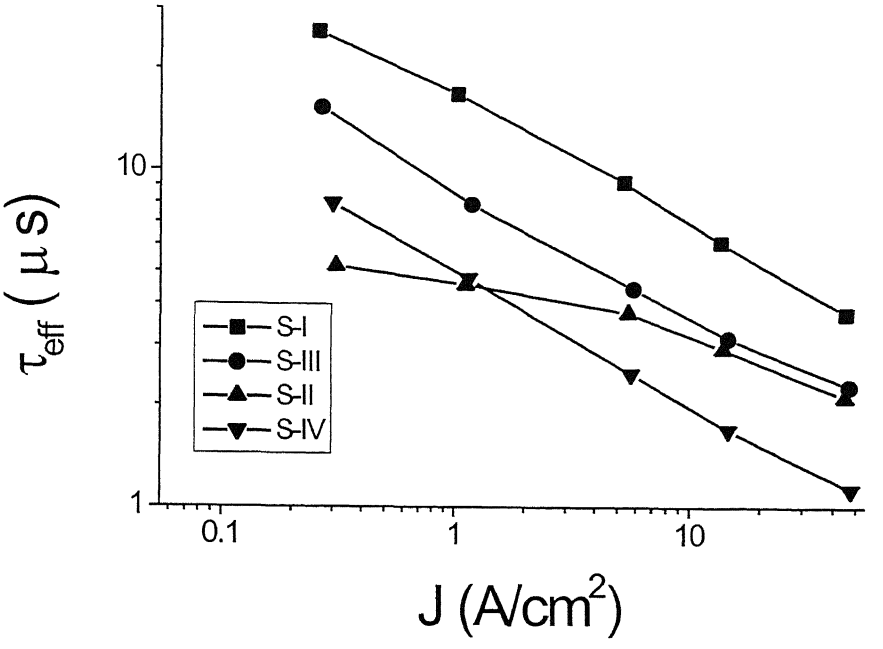


Fig. 2.18 A comparison of τ_{eff} vs J of diodes (S-I, II, III & IV)

As expected, the new structure S-IV shows better effective lifetime than that of diode S-I and diode S-III. It also compares well with diode S-II, particularly at higher current density. Fig. 2.19 and 2.20 show a comparison of current ratios I_L/I_M and I_R/I_M for the different diodes S-I to IV. The improvements in reverse recovery are 60% and 66% at low and high current densities respectively in the proposed structure with respect to conventional structure. The corresponding values of reverse recovery improvement in diode S-II are 74% and 40%. The better performance of the new structure S-IV can be attributed to improved values for both I_L/I_M and I_R/I_M ratios in the device.

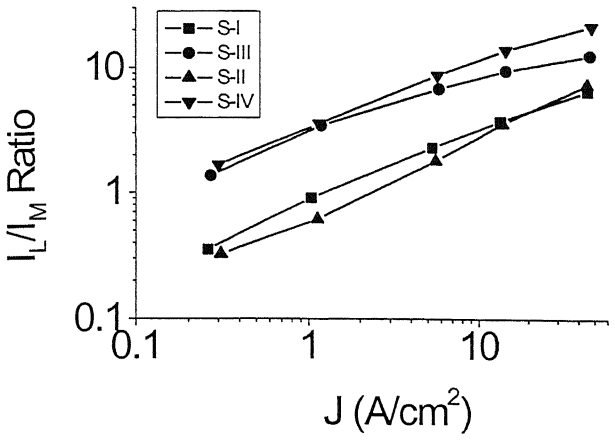


Fig. 2.19 - A comparison of I_L/I_M of diodes S-I , S-II, S-III and S-IV

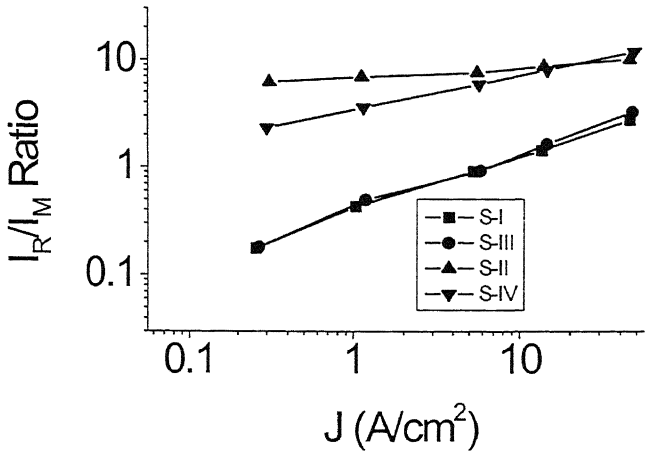


Fig. 2.20 - A comparison of I_R/I_M of diodes S-I , S-II, S-III and S-IV

The breakdown voltages of these structures have been simulated. There is no perceptible difference in the breakdown voltage of S-I, SIII and S-IV, which are more than double the breakdown voltage of S-II.

2.7 Forward '0N' Voltage

The insertion of universal contact besides resulting in improvement in reverse recovery performance is also accompanied with an improvement in forward ON voltage. This can be explained by noting that the total current flowing through the device can be expressed as

$$I = I_L + I_M + I_R = I_M \left(1 + \frac{I_L}{I_M} + \frac{I_R}{I_M}\right) \qquad (2.22)$$

Eq (2 22) implies that an increase in I_L/ I_M or the I_R/I_M ratio would result in an overall increase in the total current flowing through the device for the same applied voltage or a decrease in forward ON voltage for the same current A comparison of the simulated forward ON voltage of high breakdown voltage diodes is shown in Fig. 2.21. The voltage is the difference between the hole quasi-fermi voltage and electron quasi-fermi voltage in the forward ON state of different simulated diode structures at different current densities. The forward-on voltage of the diode S-II is the least amongst all the diodes at less than about 5 A/cm^2 and above 5 A/cm^2, the proposed diode S-IV is having the least forward ON voltage amongst all the four simulated diode structures.

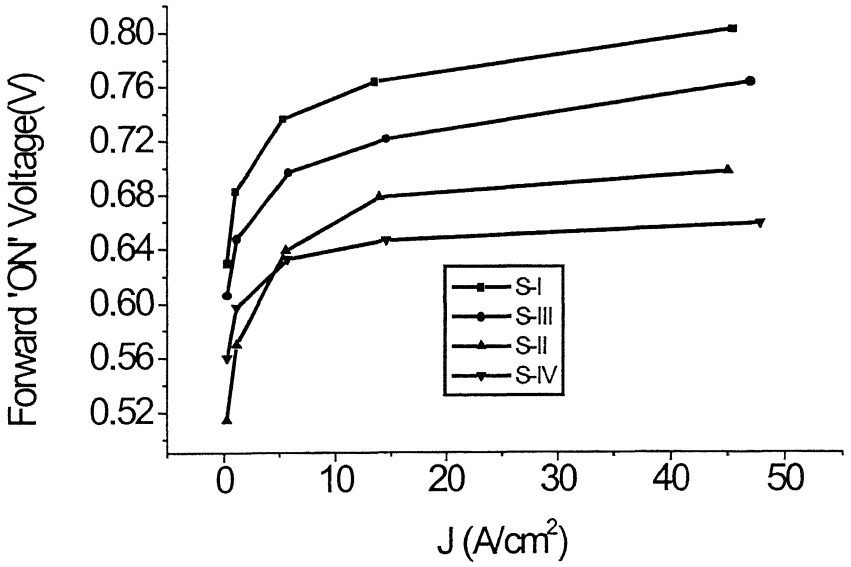
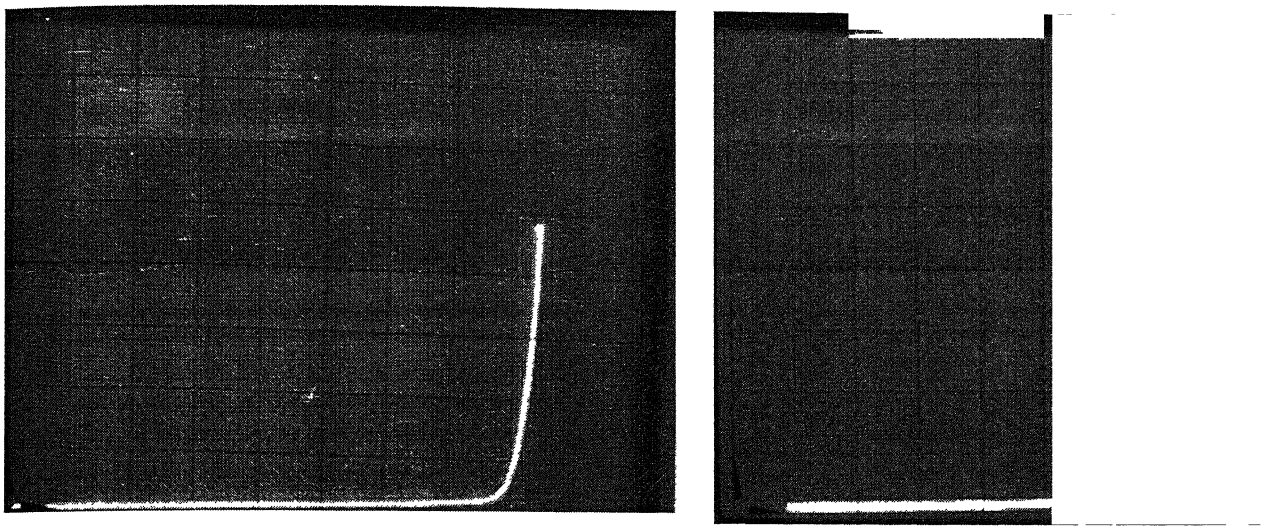


Fig. 2.21 - Forward on voltage vs current density for high voltage diode

The forward ON voltage of the diode S-III is lower by about 50 mV at 50 A/cm^2 in comparison to the conventional diode S-1. The corresponding decrease in forward ON voltage of diode S-IV is 145 mV at about 50 A/cm^2. To summarize, the incorporation of the universal contact in the p^+ region lead to improvement of switching characteristics and forward ON voltage and these improvements have been achieved without compromising the reverse blocking capability.

2.8 EXPERIMENTAL RESULTS

To verify some of the results obtained in modeling and simulation parts, diodes S-I, S-II and S-III have been fabricated. The diodes S-I and S-III have been fabricated with breakdown voltage of ~ 150 V as well of >1000V. The photograph of the breakdown voltage of low and high voltage diode is shown in Fig. 2.22 (a) and (b). The breakdown was measured at wafer level. High voltage diode could be measured up to 1000 V, though the breakdown voltage of the diode is higher than 1000V. The measured Leakage currents are given in Table 2.2.



(a) (b)

Fig. 2.22 Photograph showing breakdown voltage of S-I diodes (a) Low voltage diode (Hor. Scale 20 V/Div) (b) High voltage diode (Hor. Scale 200 V/Div)

The diode S-II has also been made in the same material as of S-III but it has breakdown voltage of ~500V due to the reach-through breakdown. The technology and process flow for the fabrication of conventional and modified diodes is described in Chapter IV. The efforts have been made to keep the material and process same for these devices so as to eliminate the possibility of lifetime variation due to extraneous account. The devices have been characterized for reverse breakdown voltage, leakage current and reverse recovery. The diode physical parameters, p^+n^+ ratio and their dc characteristics are given in Table 2.2.

Table 2.2 Details of the fabricated diodes & their dc characteristics

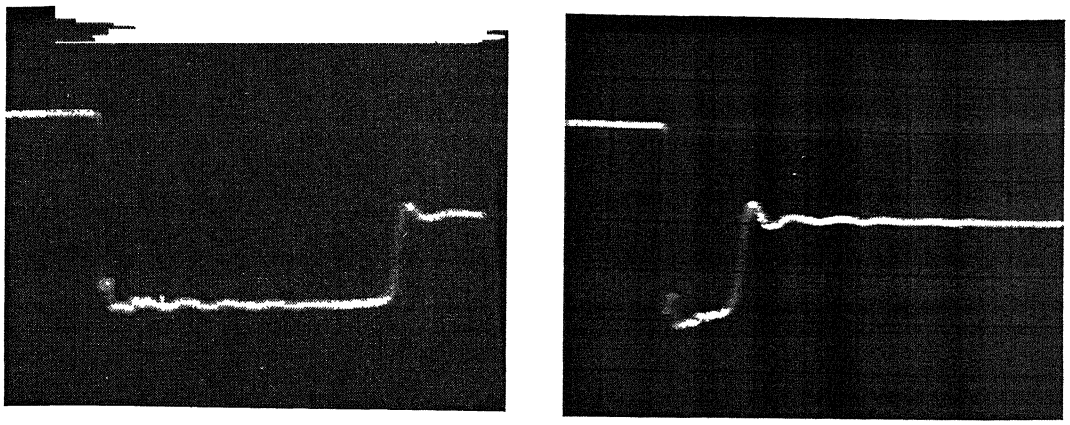
Diode	Base Resistivity And Width	P^+ diffusion	Breakdown Voltage & leakage	n^+ diffusion in p for "universal contact" (Refer Fig.2.4)
(1)Low Voltage (S-I & S-III)	nn^+ epi, n width 15 μm & Conc.1.15 x 10^{15} /cm^3	R_s 98 Ω/sq Xj = 5.4 μm ,	BV 130-155 V Leakage 100 nA at 100V	Rs=1.8 Ω/sq, X_J= 3.2 μm (P^+N^+ ·. 20 : 20 ,20.40, 20:80 μm) in S-III
(2)High Voltage (S-I & S-III)	Bulk silicon, 210 μm , & Conc. 4 x 10^{13} /cm^3, (back n^+ diff. Sur Conc 1 x 10^{19} /cm^3, x_J = 35 μm)	R_s 100Ω/sq, xj = 23.0 μm	BV >1000 V Leakage 5 μA at 1000V	Rs=5.6 Ω/sq, X_j= 7 μm (P^+N^+ :: 20 : 20 ,20:40, 20:80 μm) in S-III
(3)High Voltage (S-1 & S-II)	Bulk silicon, 175 μm , Conc ~ 4 x 10^{13} /cm^3, (back n^+ diff. Sur. Conc 1 x 10^{19} /cm^3, xj = 35 μm in S-1 only)	R_s 100Ω/sq, xj = 23.0 μm	BV ~400 – 500 V Leakage 2 μA at 400V	n^+ diff., Sur. Conc. 5 x 10^{20} /cm3 , xj = 4.48 μm p+ diff. Sur. Conc 5 x 10^{19} /cm3, xj = 3.0 μm (p+ : n+ ::20 μm : 50 μm) in S- II

The experimental setup for the measurement of reverse recovery is given in Appendix 'D'. The results for reverse recovery time, measured by keeping I_F, the forward on current and I_{REV}, the reverse switching off current equal, are shown in Table 2.3. As observed from the Table 2.3, the reverse recovery is decreasing at higher current density both in S-I and S-III. Similar results were expected from the model developed and shown by the simulation experiments. The decrease in reverse recovery in low

voltage diode is around 75%, Table 2.3. The improvement in high voltage diode is 23-30%, Table 2.4. The same order of improvement was also observed during simulation. The improvement in high voltage S-II with respect to S-I is about 70%, Table 2.5. Similar results were expected from modeling and simulation. The photographs of reverse recovery waveform for S-I and S-III are shown in Fig 2.23(a) & (b) and Fig. 2.24 (a) & (b) for low and high voltage diodes respectively.

Table 2.3 - Measured reverse recovery of low voltage diodes S-I & S-III

Diode type & I.D	Breakdown Voltage	I_F /I_{REV} (mA)	Storage time ns		Fall time ns		Reverse Recovery (τ_s + 90% of τ_f) ns		
			S-I	S-III	S-I	S-III	S-I	S-III	% Improvement
Low Voltage Diode) Base Area 0.14 x 0.14 cm^2									
S-I (1X4) Q3	155 V	10/10	1060	230	30	30	1090	260	76
		20/20	790	190	30	30	820	220	73
		30/30	680	160	30	30	710	190	73
		40/40	600	140	30	30	630	170	73
		60/60	510	110	30	30	540	140	74
		80/80	450	100	30	30	480	130	73
		90/90	425	80	30	30	455	110	76

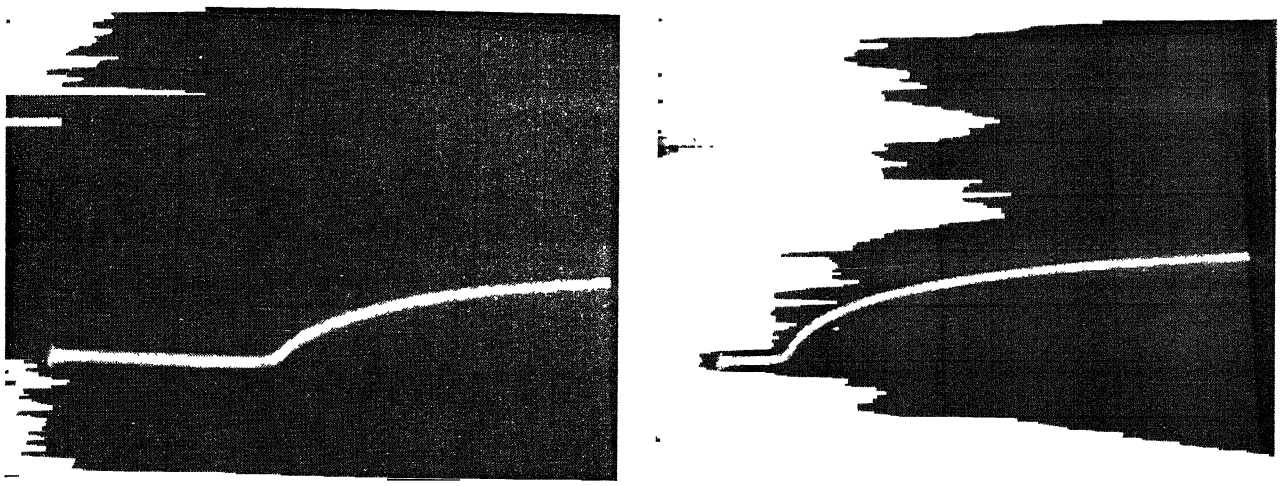


(a) (b)

Fig. 2.23 **Photograph of reverse recovery waveform of low voltage diode (a) S-I (b) S-III (Hori. Scale 100 ns/Div, Vertical Scale 20 mA/Div)**

Table 2.4 Measured reverse recovery of high voltage diode S-I & S-III

Diode type & I.D.	Breakdown Voltage	I_F/I_{REV}	Storage time μs		Fall time μs		Reverse Recovery (τ_s + 90% of τ_f) μs		
			S-I	S-III	S-I	S-III	S-I	S-III	% Improvement.
High Voltage Diode Base Area 0.1 x .1 cm^2									
S – I (R1 2X1 –Q3)	>1000 V	10/10	6	3.0	7.5	7.4	13.5	10.4	23
		20/20	4.8	2 0	7.5	7.4	12.3	9.4	23.5
		30/30	4.0	1.5	7.5	7 0	11.5	8.5	26
		40/40	3.6	1.2	7.5	6.6	11.1	7.8	30
		60/60	2.8	0 9	7.1	6.0	9.9	6.9	30
		80/80	2 4	0 8	6.8	6 0	9.2	6.8	26
		90/90	2.2	0.7	6.5	5.9	8.7	6.6	24



(a) (b)

Fig. 2.24 **Photograph of reverse recovery waveform of low voltage diode (a) S-I (b) S-III (Hori. Scale 1 μs/Div, Vertical Scale 20 mA/Div)**

Table 2.5 Measured Reverse Recovery of high voltage Diode S-I & S-II

Diode type & I.D.	Breakdown Voltage	I_F/I_{REV} (mA)	Storage time μs	Fall time μs	Reverse Recovery (τ_s + 90% of τ_f) μs	
						% Improvement.
High Voltage Diode (A comparison with Amemiya Diode)						
S – I (Device 1 X 2)	>1000 V	20/20 40/40	11.8 10.2	2 6 2.6	14.4 12.8	72 69
S - II (Device 1X2)	400-500 V	20/20	2.5 2.5	1 5 1.5	4.0 4.0	

The experimental results show an improvement of about 75% in switching performance for low voltage diodes and 23-40 % for high voltage diodes, in agreement

with the trends observed in the simulated results. The improvement in reverse recovery was accompanied by no noticeable change in the breakdown voltage.

In addition to incorporation of universal contact in the end regions, use of hetro-structures can also be potentially used to further improve the effective lifetime. By using a wide band-gap semiconductor in the middle region and suitable narrow band-gap semiconductors in the end regions, the current ratios I_L/ I_M and I_R/I_M could possibly be considerably increased leading to very low effective minority carrier lifetime in the device.

2.9 SUMMARY OF DIODE RESULTS

The use of n^+p^+ "universal contact" for improving the switching performance of power diodes was examined in detail. By incorporating the n^+p^+ "universal contact' in the end regions of a diode, an increase in the fraction of end region injected currents and significant lowering of the effective lifetime was observed. It was found that the incorporation of this modification in left region improved the reverse recovery of low voltage diodes (100 –200 V) by 77% and for high voltage (1000 V) diode by 40%. In high voltage diodes, due to large middle region thickness, the fraction of current injected into the left region is relatively less and the improvement of reverse recovery is also less as compared to low voltage diodes. The improvement for both low and high voltage diodes was found to increase with current density, this is due to the difference in voltage dependence of current injected into the left region (ideality factor ~ 1) and the middle

region (ideality factor ~ 2). The results obtained from simulation were found to be in agreement with experimental results. A new structure incorporating universal contact in both left (p^+) and right (n^+) regions of the diode has been proposed to further improve the diode's switching performance.

CHAPTER III

POWER BIPOLAR JUNCTION TRANSISTOR (BJT)

3.1 INTRODUCTION

Switching time and switching losses are primary concerns in high power applications. These two factors can significantly influence the frequency of operation and the efficiency of the circuit. Ideally, a high power switch should be able to turn-on and turn-off controllably and with minimum switching loss. The Bipolar junction transistor is an important power semiconductor device used as a switch in a wide variety of applications. The switching speed of a BJT is often limited by the excess minority charge storage in the base and collector regions of the transistor during the saturation state. The conventional methods for improving the switching frequency by reducing the lifetime of the lightly doped collector region through incorporation of impurities such as Au, Pt or by introducing radiation-induced defects have been found unsuitable for high voltage devices due to increased leakage, soft breakdown and high 'ON' state voltage [27]. Among the techniques proposed to overcome these problems, use of universal contact (UC) [2, 14] is particularly promising. The present work looks in detail at the various aspects arising out of incorporation of UC in BJTs. The UC is incorporated in the transistor by creating additional diffused regions in an otherwise conventional transistor. These diffused regions influence the minority carrier distribution, nature of minority current flow and also some other parameter such as $V_{CE(sat)}$. To study these phenomena,

an analytical model is developed and is utilized to understand the effect of universal contact on reverse recovery, $V_{CE(sat)}$ and other related issues.

3.2 REVERSE RECOVERY OF POWER BJT

Fig. 3.1 shows a schematic of a conventional bipolar junction transistor (BJT), henceforth referred as structure S-I. In the ON state, large storage of minority electrons and holes takes place in base and collector regions respectively. These minority charges must be removed during the turn-off process to restore the device to its blocking state. To speed up the reverse recovery, a reverse bias to the base-emitter junction is generally applied to enhance the turn-off process.

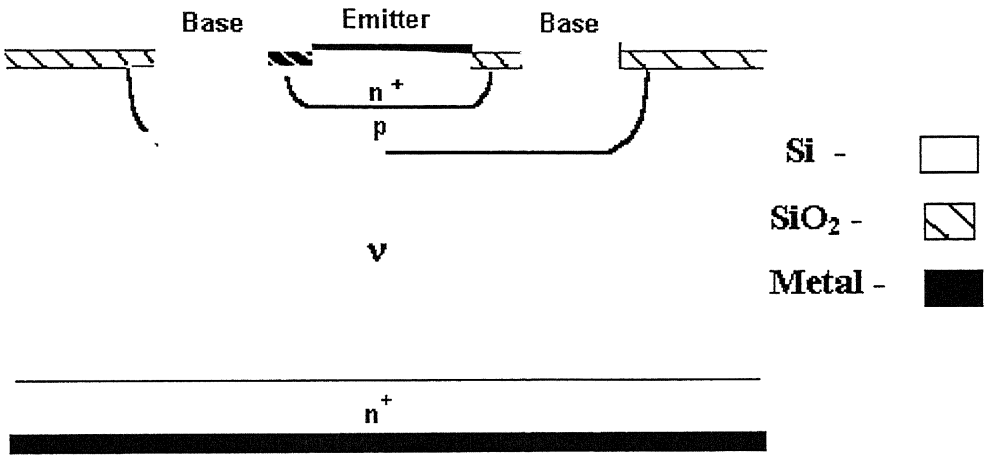


Fig. 3.1 Conventional bipolar junction transistor (S-I) showing single emitter finger between two base fingers

Fig 3.2 shows a typical base and collector current reverse recovery waveform of the transistor. These were obtained using the Silvaco simulation package [15]. The 2D simulations are based on drift-diffusion formalism and take into account the concentration dependent SRH recombination, concentration and field dependent mobility,

band gap narrowing and Auger effects. To put off the transistor, reverse bias is applied at the instant t_0. The base current immediately changes to reverse current, J_{BR} with a magnitude depending upon the supply voltage and series resistance. The constant collector current continues flowing in the same direction till the time t_1. After t_1, collector current starts decreasing. The constant collector current phase and the 90% of the fall time are defined as the total reverse recovery time (τ_{rr}).

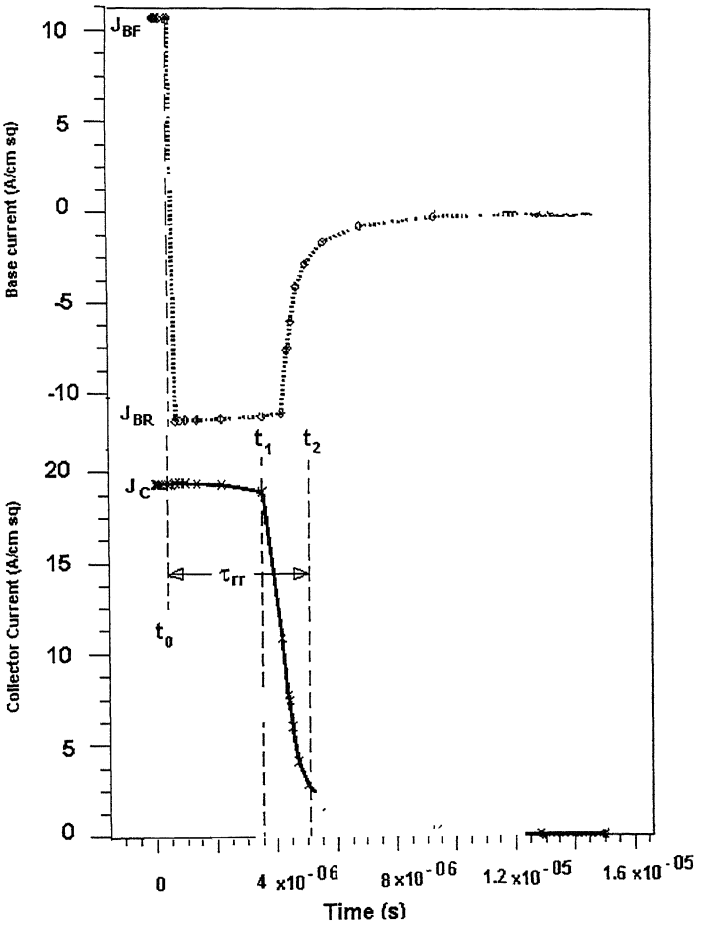


Fig. 3.2 Base and collector current waveforms during turn-off

The excess electron and hole concentration profiles at 2 μs, 4 μs and at 6 μs in the different phases of the reverse recovery waveform are shown in Fig. 3.3 [28]. As seen

from the Fig. 3.3, there is large minority charge concentration in the collector region at 2 μs though a voltage to switch off the transistor was applied at $t_0 = 0.5$ μs. Because of this excess charge, the collector current remains constant.

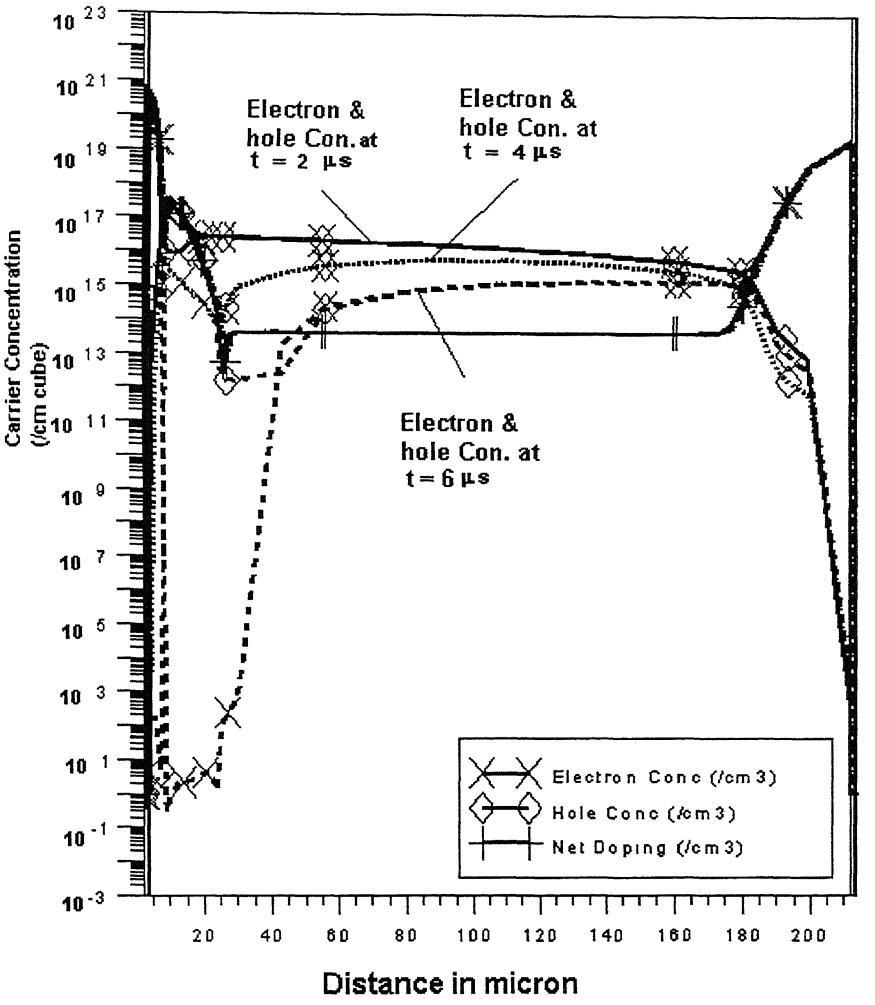


Fig. 3.3 Carrier concentration during reverse recovery in hard switching

The potentials at these different phases of reverse recovery time are also shown in Fig. 3.4. As seen from the Fig. 3.4, the voltage drop at 2 μs is constant through out the device and is less than 0.5V. At 4 μs, the voltage has risen to 1V after the depletion

region has formed near the base-collector region. At 6 μs the voltage has risen to 10V and there is still excess charge left out inside the device. This remaining charge give rise to long fall time tail observed in high voltage devices.

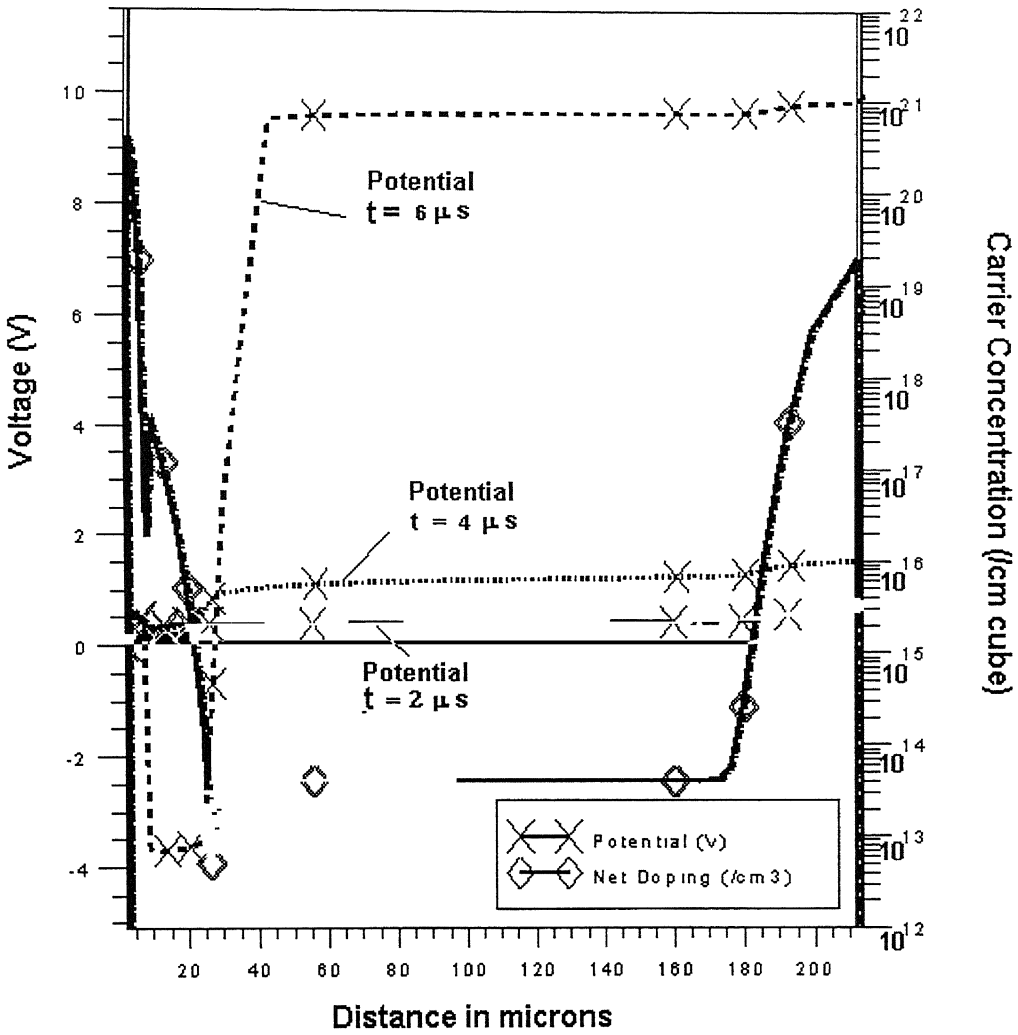


Fig. 3.4 Potential drop in reverse recovery during hard switching

The reverse recovery time (τ_{rr}) of the transistor is intimately related to the effective minority carrier lifetime (τ_{eff}) in the device defined as

$$\tau_{eff} = \frac{Q}{I_B} \qquad (3.1)$$

Where Q is the total minority charge stored in emitter, base and collector regions and I_B is the base terminal current. As an example Fig. 3 5 shows a comparison of reverse recovery time for a BJT of breakdown voltage >1000 Volts with the effective minority carrier lifetime obtained using 2D numerical simulations of the transistor.

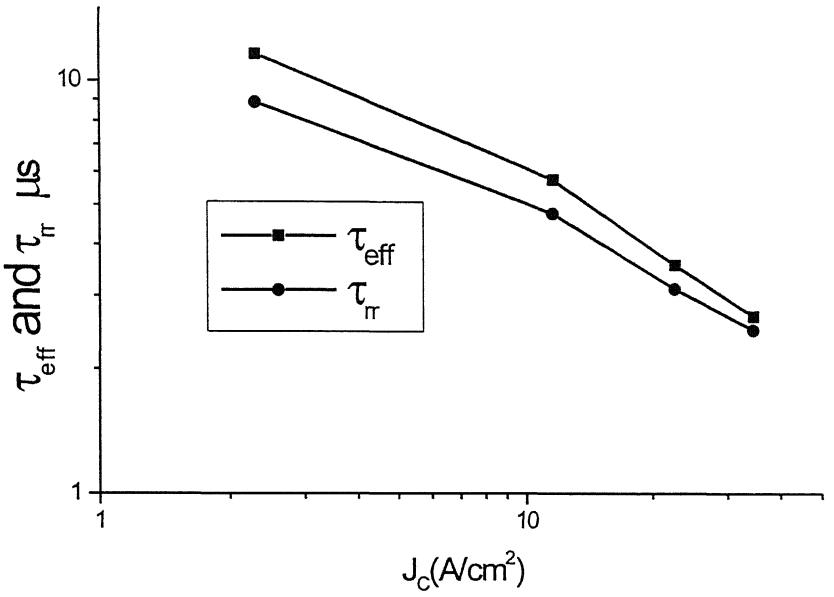


Fig. 3.5 **A comparison of effective lifetime with reverse recovery time of BJT of >1000 V**

It can be seen from Fig. 3.5 that the effective lifetime tracks the reverse recovery time quite well so that it can be used as a simple and easy to model parameter for study.

3.3 ANALYTICAL MODEL - EFFECTIVE LIFETIME

The effective lifetime can be related to other device parameters by noting that in the ON state, the transistor is in saturation so that both the base-emitter and base-collector junctions are forward biased. As a result, minority charges are stored in the emitter (Q_{hE}), base (Q_{eB}) and collector (Q_{hC}) regions so that Eq. (3.1) can be re-written as

$$\tau_{eff} = \frac{Q_{hC}}{I_B}\left(1+\frac{Q_{hE}}{Q_{hC}}+\frac{Q_{eB}}{Q_{hC}}\right) \qquad (3.2)$$

Since the doping in the emitter region is much higher as compared to doping in the collector region, $Q_{hE} << Q_{hC}$, so that Eq. (3.2) may be simplified to

$$\tau_{eff} = \frac{Q_{hC}}{I_B}(1+\frac{Q_{eB}}{Q_{hC}}) \qquad (3.3)$$

If I_{hC} is the hole current injected into the collector, then

$$Q_{hc} = \tau_0 \times I_{hC} \qquad (3.4)$$

Where τ_0 is the hole lifetime in the collector region. This allows Eq. (3.3) to be expressed as

$$\tau_{eff} = \tau_0 \frac{I_{hC}}{I_B}(1+\frac{Q_{eB}}{Q_{hC}}) \qquad (3.5)$$

Since the doping in the base is often much higher than that in the collector and base width is also much smaller than collector thickness, it can be assumed that $Q_{eB} << Q_{hC}$, so that

$$\tau_{eff} = \tau_0 \frac{I_{hC}}{I_B} \qquad (3.6)$$

Equation (3.6) indicates that there are two ways of decreasing the effective lifetime. One is by reducing the bulk lifetime τ_0, by introducing the life killing elements Au, Pt etc and the other is by reducing the fraction $(\frac{I_{hC}}{I_B})$ of current that results from recombination in the collector region to base terminal current. Eq. (3.6) can be cast into an alternative form by noting that the total base current I_B can be expressed as sum of three components; hole current injected into the emitter, hole recombination current in base region and hole current injected into the collector. For transistors with moderate or high current gain, the component of current due to injection of holes into the emitter is much smaller than the other two components in saturation state so that, $I_B \approx I_{hB} + I_{hC}$.

This allows Eq. (3.6) to be re-written as

$$\tau_{eff} \cong \tau_0 \frac{1}{\left(1+\frac{I_{hB}}{I_{hC}}\right)} \qquad (3.7)$$

Eq. (3.7) can be re-written in a more instructive form as

$$\frac{1}{\tau_{eff}} \cong \frac{1}{\tau_0} + \frac{1}{\tau_{hB}} \qquad (3.8)$$

Where $\tau_{hB} = \tau_0 \left(\frac{I_{hC}}{I_{hB}} \right)$ Eq. (3.8) shows that effective lifetime can also be decreased by reducing the time constant τ_{hB} by increasing the hole recombination current into the base relative to hole current injected into the collector. The hole current in the base can be viewed as consisting of two components; one due to recombination in the intrinsic base region (I_{hBi}) and the other due to recombination with electrons injected by the collector into the extrinsic base region (I_{hBx}). This allows the time constant τ_{hB} to be decomposed into two components:

$$\frac{1}{\tau_{hB}} \cong \frac{1}{\tau_{hBi}} + \frac{1}{\tau_{hBx}} \qquad (3.9)$$

Where $\tau_{hBi} = \tau_0 \frac{I_{hC}}{I_{hBi}}$ is the lifetime in the intrinsic base and $\tau_{hBx} = \tau_0 \frac{I_{hC}}{I_{hBx}}$ is the lifetime in the extrinsic base region.

The base current component I_{hBx} is normally small because of the small electron recombination velocity of the p^+p base ohmic contact so that time constant τ_{hBx} is large. However, if the p^+p base contact is replaced by the n^+p^+ universal contact as shown inside the base of the BJT of Fig. 3.6, henceforth called structure S-II, the electron current injected into the extrinsic base is expected to increase considerably resulting in sharp decrease in τ_{hBx} and the overall effective recombination lifetime.

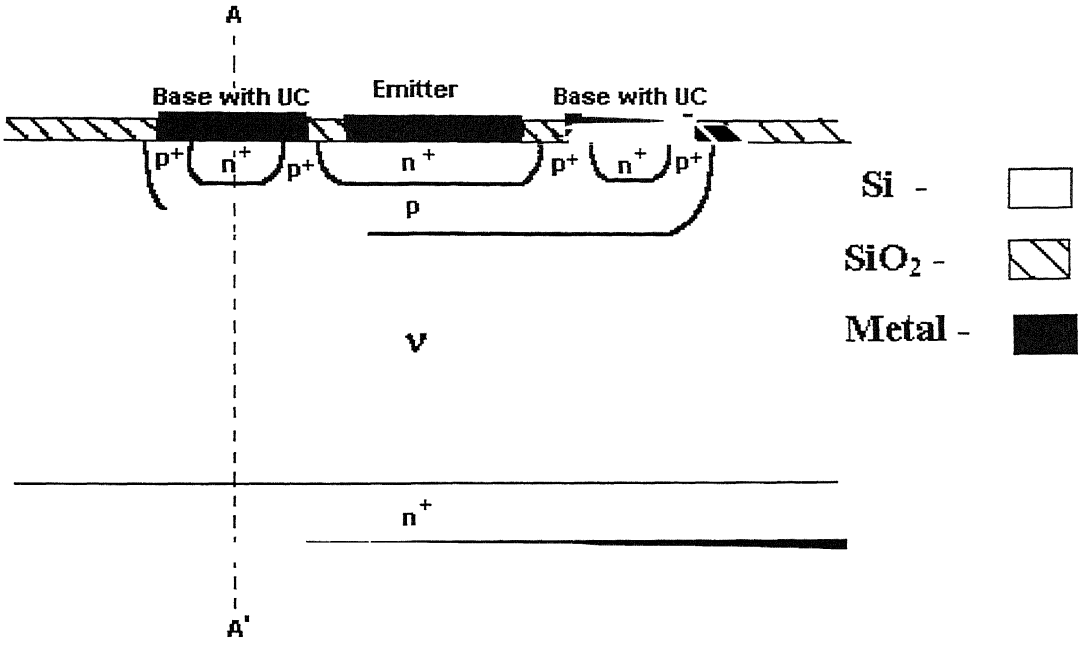


Fig. 3.6 Bipolar junction transistor (S-II) including single emitter finger and two base fingers with universal contact

This method of reduction in effective lifetime is similar to the improvement in reverse recovery obtained by connecting a Schottky diode externally between base and collector. The use of Schottky diode with lower turn-on voltage allows base current to be diverted from collector region of the transistor where recombination lifetime is high to the Schottky diode which has zero effective minority carrier lifetime. In the present approach also, the base current is diverted from collector region to extrinsic base region where effective recombination lifetime is low due to presence of universal contact. Although the principle is essentially same, the present approach has the benefit of being applicable to high voltages also and also promises to have lower silicon area.

The discussion so far has brought about the importance of low value of the time constant τ_{hBx} or equivalently the ratio $\frac{I_{hC}}{I_{hBx}}$ for improving the effective lifetime. We next discuss the important factors that impact the ratio of hole current injected into the collector and the electron current injected into the extrinsic base region.

3.4 ANALYTICAL MODEL - DEPENDENCE OF EFFECTIVE LIFETIME ON DEVICE PARAMETERS

Fig. 3.7 shows a 1D view of the device in the extrinsic base in the region where n^+ diffusion in p-diffused base as part of universal contact has been made.

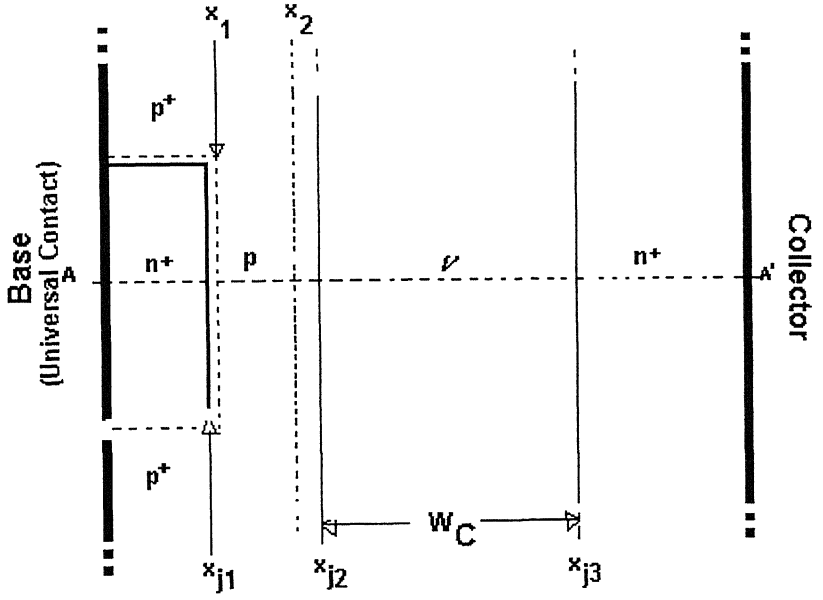


Fig. 3.7 **A one-dimensional view of the transistor incorporating universal contact at A-A' of Fig. 3.6.**

The x_{j1}, x_{j2} and x_{j3} are the metallurgical junctions in front n^+p "universal contact", pυ junction and back $υn^+$ contact. The x_1 and x_2 are the depletion edges of n^+p and pυ junctions inside the p diffused region. Analogous to PIN [29] diode, the collector voltage (V_{BC}) in saturation can be expressed as the sum of three components as follows:

$$V_{BC} = V_{BC1} + V_{BC2} + V_{BC3} \qquad (3.10)$$

Where V_{BC1} is the voltage drop at x_{j2}, V_{BC2} is the voltage drop in the collector region in saturation and V_{BC3} is the voltage drop at x_{j3}.

The hole current, I_{hBx}, which is identical to the electron current injected by the collector into the base, can be expressed

$$I_{hBx} = \frac{q^2 n_i^2 D_n \exp\left(\frac{qV_{BC1}}{kT}\right)}{Q_p} \varsigma (A_{BC} - A_E) \qquad (3.11)$$

Where A_{BC} is the base-collector area, and A_E is the emitter area, $\varsigma = \frac{A_{N^+}}{(A_{BC} - A_E)}$, is the fraction of extrinsic base area occupied by n^+ part of the universal contact and A_N^+, is the area of n^+ in the universal contact.

Defining a factor $\eta_B = \frac{V_{BC}}{V_{BC1}}$, equation (3.11) may be written as

$$I_{hBx} = \frac{q^2 n_i^2 D_n \exp\left(\frac{qV_{BC}}{\eta_B kT}\right)}{Q_p} \varsigma (A_{BC} - A_E) \qquad (3.12)$$

For simplicity, we assume that when junction is forward biased $x_2 = x_{j2}$ and low level injection conditions prevail so that $Q_p = q\int_{x_1}^{x_{j2}} N_a(x)\,dx$. To avoid reach-through prior to onset of breakdown, we require that at breakdown $(x_{j2} - x_1) > 0$. Taking E_C as the critical field, we obtain the condition

$$\frac{q}{\varepsilon_s}\int_{x_1}^{x_{j2}} N_a dx > E_C \qquad (3.13)$$
$$or\ Q_p > \varepsilon_s E_C$$

Defining $f_B = \frac{Q_p}{\varepsilon_S E_C}$, allows Eq. (3.12) to be re-written as

$$I_{hBx} = \frac{q^2 n_i^2 D_n \exp\left(\frac{qV_{BC}}{\eta_B kT}\right)}{f_B \varepsilon_s E_C} \varsigma (A_{BC} - A_E) \qquad (3.14)$$

The factor f_B represents a safety factor in the sense that for $f_B > 1$, the charge, Q_p under the universal contact is large enough to prevent onset of reach-through prior to onset of avalanche breakdown. On the other hand if $f_B < 1$, then the reverse blocking voltage would be determined primarily by the occurrence of reach-through.

The minority carrier current I_{hC} can be modeled as recombination current in the collector region and written as

$$I_{hC} = qn_i \frac{W_C}{\tau_0} \exp\left(\frac{qV_{BC}}{\eta_C kT}\right) A_{BC} \qquad (3.15)$$

Where $\eta_C = \frac{V_{BC2}}{V_{BC}}$ is the ideality factor of the recombination current in the collector region. The ratio I_{hBx}/I_{hC} can now be obtained using Eq. (3.14) and Eq. (3.15) as

$$\frac{I_{hBx}}{I_{hC}} = q n_i D_n \frac{\tau_0}{W_C} \frac{\exp\left(\frac{qV_{BC}}{kT}\left(\frac{1}{\eta_B} - \frac{1}{\eta_C}\right)\right)}{f_B \varepsilon_s E_C} \varsigma \frac{(A_{BC} - A_E)}{A_{BC}} \qquad (3.16)$$

The total base current J_B may be written in terms of its ideality factor n as

$$J_B = J_O \exp\left(\frac{qV_{BC}}{nkT}\right) \qquad (3.17)$$

Equation (3.17) can be used to re-write Eq (3.16) as

$$\frac{I_{hBx}}{I_{hC}} = C_B \frac{\tau_0}{W_C} \frac{J_B^{\alpha_{BC}}}{f_B} \qquad (3.18)$$

Where $\alpha_{BC} = n \times \frac{\eta_C - \eta_B}{\eta_C \eta_B}$ and $C_B = \frac{q\, n_i\, D_n}{\varepsilon_s E_C J_0^{\alpha_{BC}}} \varsigma \frac{(A_{BC} - A_E)}{A_{BC}}$

Substitution of Eq. (3.18) and corresponding value of $\frac{I_{hC}}{I_{hBi}}$ in Eq. (3.7), we obtain

$$\frac{1}{\tau_{eff}} \cong \frac{1}{\tau_o} + \frac{1}{\tau_{hBi}} + \frac{1}{\tau_{hBx}} \qquad (3.19)$$

Where $\tau_{hBx}^{-1} = C_B \dfrac{J_B^{\alpha_{BC}}}{f_B W_C}$

Eq. (3.19) can be used to explain several important features regarding the effective minority carrier lifetime and therefore the switching speed of the transistors with universal contact. For example Eq. (3.19) shows that the effective lifetime will decrease with increase in base or collector current density. The reason for this is due to the different ideality factors of the current injected into the collector and extrinsic base region. The minority hole current in the collector region increases as $\exp(qV_{BC}/2kT)$ due to high level injection in the collector region, while the current injected into the base increases $\exp(qV_{BC}/kT)$ due to low level injection condition, causing the ratio I_{hBx}/I_{hC} to increase with increase in bias or with increase in current density. Eq. (3.19) also indicates that the effective lifetime will increase as breakdown voltage increases. The reason for this is that increase in the breakdown requires increase of the thickness W_C of the collector region, which decreases the ratio of I_{hBx}/I_{hC}. Eq. (3.19) also shows that a decrease in safety factor f_B will improve I_{hBx}/I_{hC}. In fact, f_B may be made less than unity indicating onset of reach-through prior to avalanche breakdown. This illustrates a new mechanism whereby the reverse blocking characteristics can be traded with the switching characteristics.

Along with reverse recovery time and breakdown voltage, the collector-emitter voltage in ON state is another very important transistor characteristics. The insertion of universal contact in the extrinsic base region is expected to have influence on this parameter. A simple analytical model is described in the next section.

3.5 ANALYSIS OF 'ON' STATE-VOLTAGE

The collector-emitter voltage in the ON state can be expressed as

$$V_{CE(sat)} = V_{CE(sat)}^{intrinsic} + I_C(R_C + R_E) \qquad (3.20)$$

Where the first term represents the intrinsic collector-emitter voltage and the second term represents the voltage drop in the parasitic collector resistance R_C and the emitter resistance R_E. A model for the first term is developed first, followed by a model for the second term.

An expression for intrinsic collector-emitter voltage can be easily obtained from Ebers-Moll [8] model:

$$V_{CE(sat)} = V_T \ln \frac{\frac{1}{\alpha_R} + \frac{I_C}{I_B}\left(\frac{1}{\beta_R}\right)}{1 - \frac{I_C}{I_B}\left(\frac{1}{\beta_F}\right)} \qquad (3.21)$$

Where β_F and β_R are current gains in forward and reverse active modes respectively. I_C/I_B is the forced β in saturation. The insertion of universal contact in the

extrinsic base region leaves the forward current gain, β_F unchanged but reduces the reverse current gain, β_R. The change in reverse current gain β_R can be explained by noting that

$$\beta_R = \frac{I_E}{I_B} = \frac{I_E}{I_{hC}} \frac{I_{hC}}{I_B} \tag{3.22}$$

Defining injection efficiency (γ_C) of the collector-base junction as

$$\gamma_C = \frac{J_E}{J_{hC} + J_E} \tag{3.23}$$

allows Eq. (3.22) to be re-written as

$$\beta_R = \frac{A_E}{A_{BC}} \frac{1}{\gamma_C^{-1} - 1} \frac{I_{hC}}{I_B} \tag{3.24}$$

Since the first two factors are the same in the normal and modified transistor, Eq. (3.24) shows that the change in β_R is directly related to the ratio $\frac{I_{hC}}{I_B}$. This means that as the ratio $\frac{I_{hC}}{I_B}$ decreases due to the incorporation of "universal contact", β_R will also be reduced leading to an increase in collector-emitter voltage in saturation. However, due to the logarithmic dependence of the voltage on current gain, the increase in voltage is expected to be small.

In the second term of Eq. (3.20), the contribution of the emitter resistance on the ON state voltage would remain unchanged as a result of insertion of universal contact

because the emitter resistance is unaffected. Similarly, in the absence of conductivity modulation in the collector region, the collector resistance would also remain unchanged. This would be true for transistors designed for low voltage operation where high-level injection condition in the collector may not occur. However, for high voltage transistors, high level injection does occur and insertion of universal contact by altering current distribution is expected to result in a modification of collector resistance.

As long as high-level injection conditions prevail in the entire collector region, the collector resistance and the voltage drop across it remain small due to conductivity modulation. However, as collector current density (and therefore base current density for a constant I_C /I_B ratio) increases, the region where conductivity modulation occurs begins to shrink leaving behind a portion of high resistance collector layer [30]. The voltage drop across this neutral collector region result in a sharp increase in collector-emitter voltage. The voltage drop in un-modulated part of the collector region is given by

$$V_U = \frac{J_C (W_C - W_M)}{q\mu_n N_D} \qquad (3.25)$$

The modulated portion of the collector region W_M, can be expressed as

$$W_M = \frac{2qD_n p(0)}{J_C} \qquad (3.26)$$

Since the hole density, p (0), at the collector-base junction is directly proportional to recombination current in collector region, J_{hC}, Eq. (26) can be written as

$$W_M = a\frac{I_{hC}}{I_C} \tag{3.27}$$

Where 'a' is a constant. Use of Eq. (3.26) allows Eq. (3.25) to be expressed as

$$V_U \propto \frac{J_C}{N_D}\left[W_C - a\frac{I_B}{I_C}\times\frac{I_{hC}}{I_B}\right] \tag{3.28}$$

Eq. (3.28) is valid only after the un-modulated region of collector begins to form. This would occur when

$$\frac{I_{hC}}{I_B} < \frac{W_C}{a I_B/I_C} \tag{3.29}$$

Since the incorporation of universal contact results in a decrease in fraction of hole current injected into the collector, the sharp increase in collector-emitter voltage is expected to occur at lesser collector current density as compared to the conventional transistor.

The analytical models developed in this section provide insight into important factors affecting different characteristics of the transistor. The next section describes an elaboration of these results obtained using 2D numerical simulation of the transistors.

3.6 SIMULATION RESULTS

To study the effect of incorporation of "universal contact" on transistor's characteristics, 2D numerical simulation were carried out. The simulations are based on

drift-diffusion formalism and take into account concentration dependent SRH recombination, concentration and field dependent mobility, band gap narrowing and Auger effect. A transistor with inter-digitated base–emitter geometry was chosen for simulations. This configuration has large extrinsic base region where the universal contact could easily be incorporated. For simulation purpose, only half of an emitter finger and a single base finger as shown in Fig. 3.8 were taken. The structure of conventional transistor S-I is same as structure of transistor S-II shown in Fig. 3.8 except that in the former, there is no universal contact in the extrinsic base region. Two different kinds of BJT devices, one with relatively low BV_{CBO} of ~150 Volts and another with BV_{CBO} exceeding 1000 Volts were chosen for study.

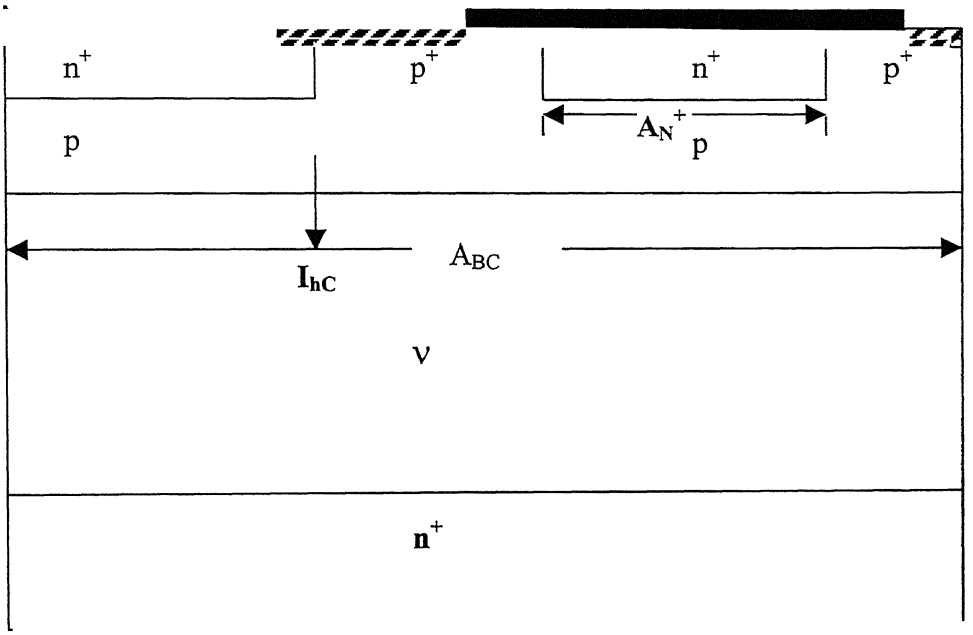


Fig. 3.8 **Transistor structure (S-II) consisting of half of emitter finger and single base finger**

The description of the low voltage transistor including surface and bulk concentration, junction depths etc is given in Table 3.1. Transistor geometry with half emitter finger width of 50 μm and a base finger width of 80 μm was taken.

Table 3.1- Details of parameters of simulated low voltage transistor

Device	Base Resistivity/ Doping and Epi-thickness	p diffusion	p^+ diffusion	n^+ diffusion in emitter & in "universal contact"	Material Lifetime τ_{n0} and τ_{p0}
Low Voltage (100-155 V)	3.4 – 4.6 Ω-cm, 1.15e15 /cm^3, 15 μm nn^+ Epitaxial Substrate thickness 280 μm	Xj=5 7 μm, Surface Conc. 2e18, gaussian profile	Xj=1.6 μm, Surface Con 2.0e19	Xj=3.0 μm, Surface Con. 4.0e20, gaussian profile, n^+:p^+ :: 40 μm:, 40 μm.	2.6 μs

In structure S-II, universal contact was incorporated with a n+/p+ ratio of 1:1. The Gummel plots obtained from simulations were found to be identical for both the transistor structures with a current gain of 80 at a collector current density of 100 A/cm^2. This is expected because the universal contact in the extrinsic base region will make a difference only when the collector-base junction is forward biased. The switching characteristics of the two structures were simulated by abruptly switching the base voltage in such a way that the forward and initial values of reverse base currents were identical. Reverse recovery time, defined as the sum of storage and 90% of fall times were extracted from the waveforms of the collector/base currents and studied as a function of collector current density. In these simulations, the ratio of collector to base

currents in the ON state was kept at a fixed value of 10. Fig. 3.9 shows a comparison of reverse recovery time for the two structures.

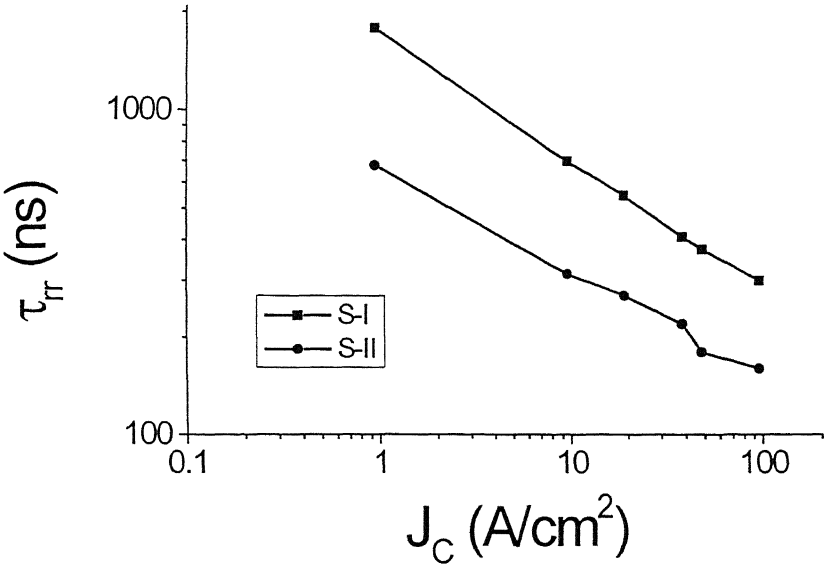


Fig. 3.9 **Reverse recovery vs Jc of low voltage transistors S-I and S-II**

The reverse recovery time decreases with increase in collector current density in accordance with the predictions of the model developed earlier. The reverse recovery time of BJT S-II is significantly shorter than that of the conventional BJT S-I with an improvement of 62.2% at a collector current density of 1 A/cm^2 and 47% at about 100 A/cm^2. Effective minority carrier lifetime was also extracted from the simulations using the definition given in Eq. 3.1. A plot of τ_{eff} versus J_C for the two structures is shown in Fig. 3.10. τ_{eff} for BJT S-II is lower by 73.8% at about 1 A/cm^2 and 56% at about 100 A/cm^2.

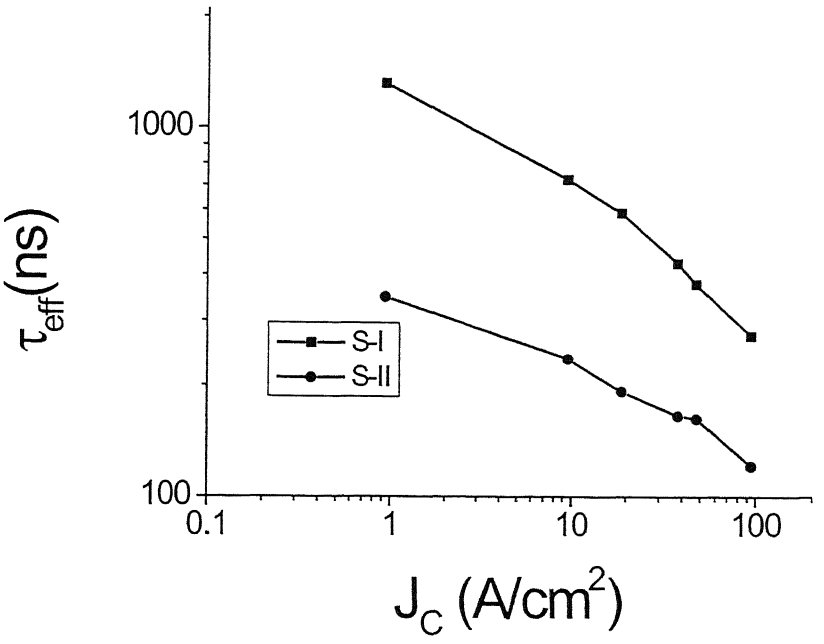


Fig. 3.10 τ_{eff} **vs** J_C **of low voltage transistors S-I and S-II**

These results are in general agreement with those of the reverse recovery time. The improvement in effective minority carrier lifetime as a result of introduction of universal contact is due to reduction in time constant τ_{hB} in structure S-II. A plot of current ratio I_{hC}/I_B is shown in Fig. 3.11. It is clear from the figure that the hole current injected into the collector is significantly reduced in structure S-II, thereby implying less minority charge storage and improved reverse recovery.

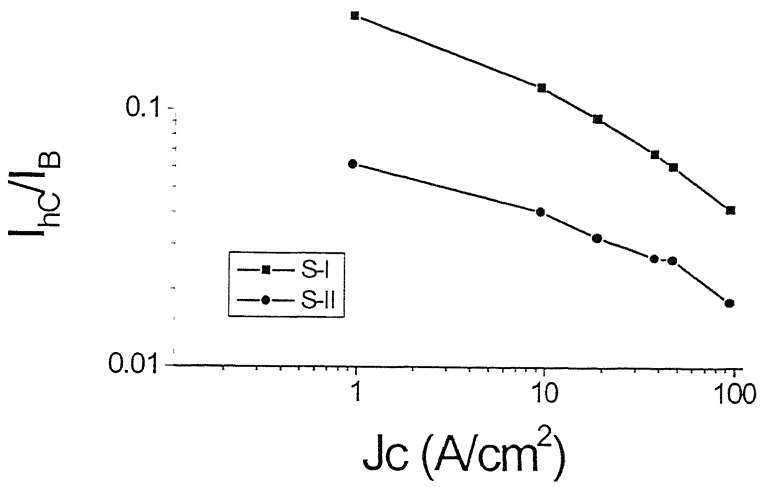


Fig. 3.11 I_{hC}/I_B **ratio vs** J_C **for low voltage transistors S-I and S-II**

As discussed earlier, the improvement in reverse recovery as a result incorporation of universal contact is accompanied with an increase in collector-emitter voltage in the ON state.

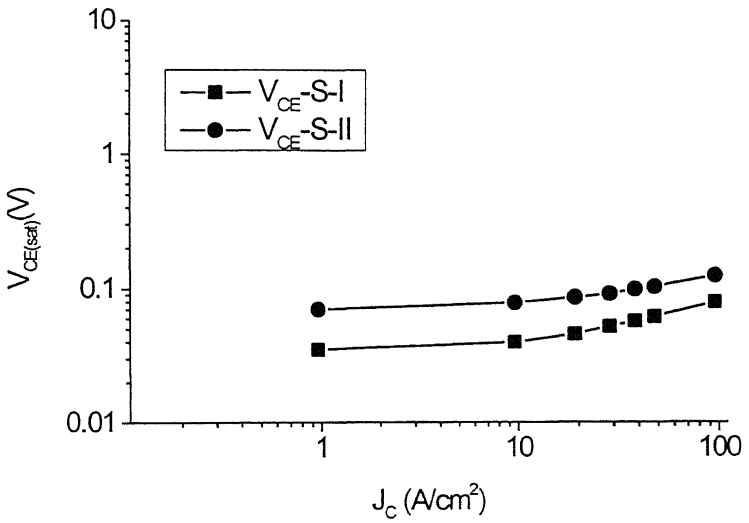


Fig. 3.12 $V_{CE(sat)}$ **vs** J_C **at** $\frac{I_C}{I_B}$=10 **of low voltage transistors S-I and S-II**

Fig. 3.12 shows a comparison of ON state voltage for the two transistor structures for an over drive current ratio of $\frac{I_C}{I_B} = 10$. The ON state voltage of BJT S-II increases by 30-50 mV in comparison to BJT S-I. As discussed earlier, the increase in ON state voltage is due to reduced value of current gain in the reverse active mode. The current gain in the reverse active mode, for the two BJT structures are shown in Fig. 3.13.

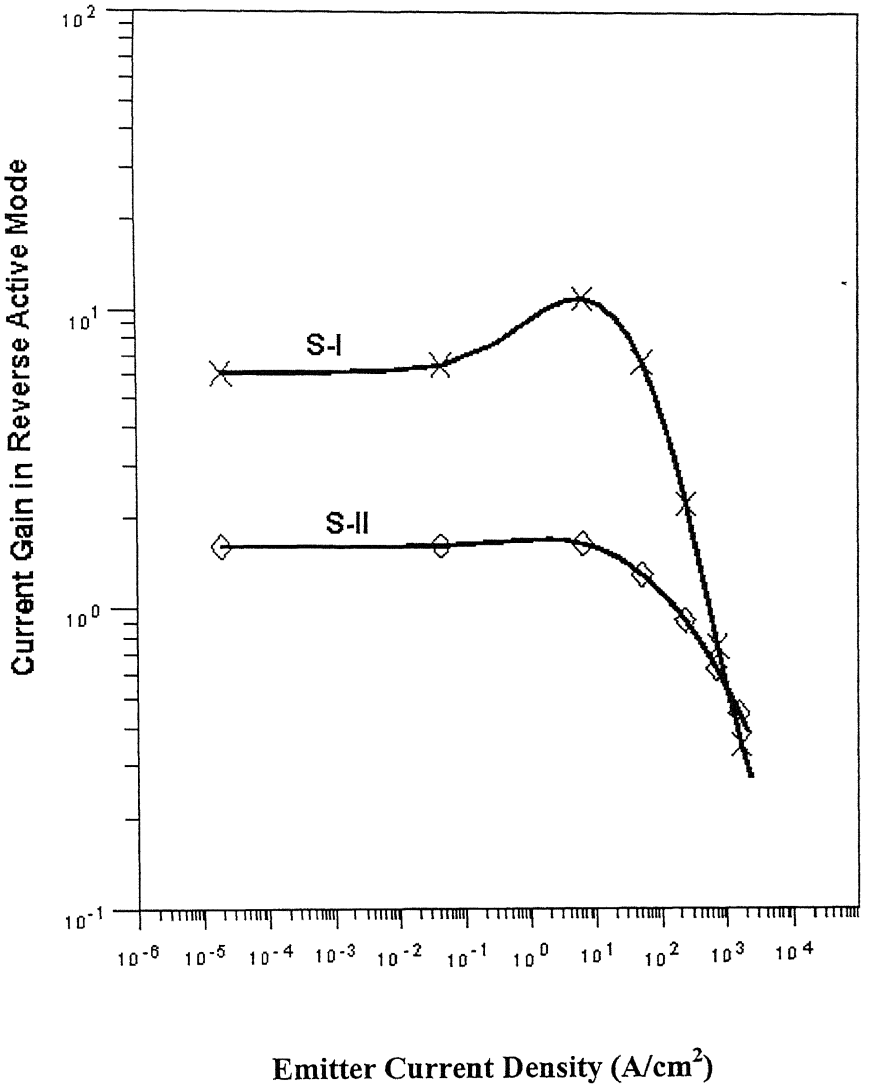


Fig. 3.13 Current gain in reverse active mode of S-I and S-II

As can be seen, the current gain reduces from approximately 6 to 1.5 as a result of insertion of universal contact. Substitution of these values in Eq. (3.21) predicts a difference of 28mV in the ON state voltage of the two transistors in general agreement with the simulated values.

In order to estimate the impact of insertion of universal contact in transistors with high breakdown voltage, BJT with doping and other parameters suitable for operation of BV_{CBO} larger than 1000 Volts was studied. Transistor structures S-I and S-II with description given in Table 3.2 and geometry with half emitter finger width of 100 μm and base finger width of 150 μm were simulated.

Table 3.2 Details of parameters of simulated high voltage transistor

Device	Bulk Resistivity/ Doping and Collector width	p diffusion in base	p^+ diffusion in base for p^+	n^+ Diffusion in emitter and for "universal contact"	n^+ Back diffusion	Material lifetime parameter τ_{n0} & τ_{p0}
High Voltage Transistor Structure	100 Ω-cm, 4e13 /cm^3, W_C = 150 μm,	Xj=23 μm, Surface Conc.6.7e17 gaussian profile	Xj =1.0 μm, Surface Con. Erfc 4.0e19	Xj=7.0 μm, Surface Con. 4.0e20, width 80 μm	Xj=35.0 μm Surface Concentration 6.0e19	20 μs

Unlike their low voltage counterparts, the I_C-V_{CE} curves for S-I and S-II high voltage transistor show some differences. Fig. 3.14 shows that there are no difference at large values of collector-emitter voltage but the collector currents for the two transistors begin to differ as the voltage gets smaller. The structure S-II is characterized by an early onset of quasi-saturation effect.

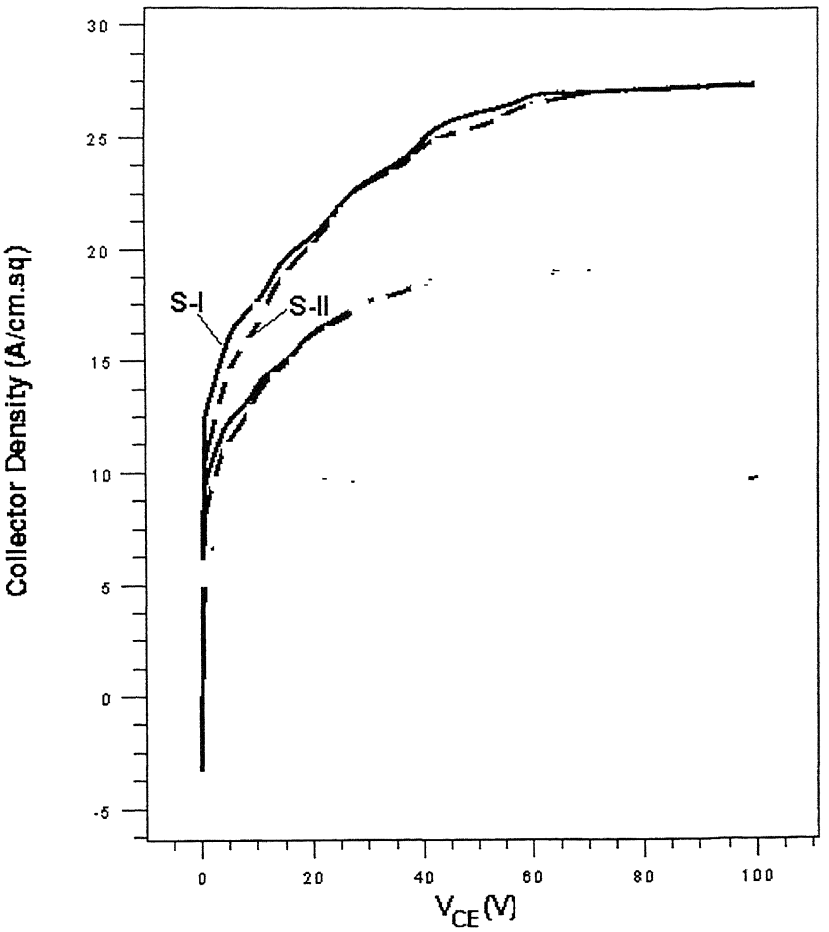


Fig. 3.14 **I_C – V_{CE} characteristics of high voltage transistor S-I and S-II**

This, as explained earlier, is due to reduced hole injection into the collector. Fig 3.15 shows a comparison of reverse recovery time for the two structures. The current ratio I_C/I_B was maintained at 2 for all the collector current densities.

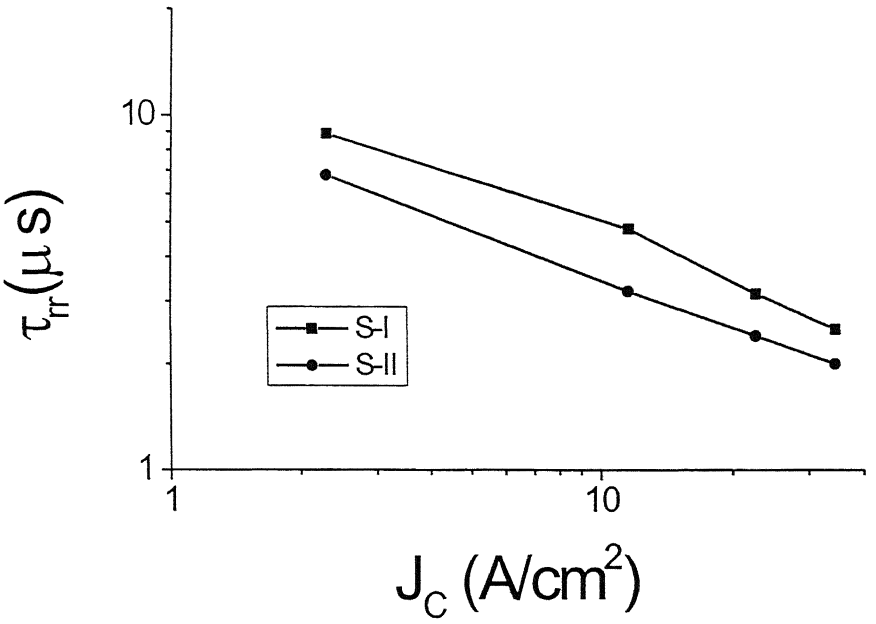


Fig. 3.15 Reverse recovery (τ_{rr}) vs J_C of high voltage transistors S-I and S-II

The improvement in reverse recovery for S-II is again noticeable though the magnitude is less being about 23.6% at 2 A/cm^2 and 20 % at 40 A/cm^2. The improvements in effective minority carrier lifetimes are also similar. Fig. 3.16 shows that τ_{eff} decreases by 30% at about 2 A/cm^2 and 28% at about 40 A/cm^2.

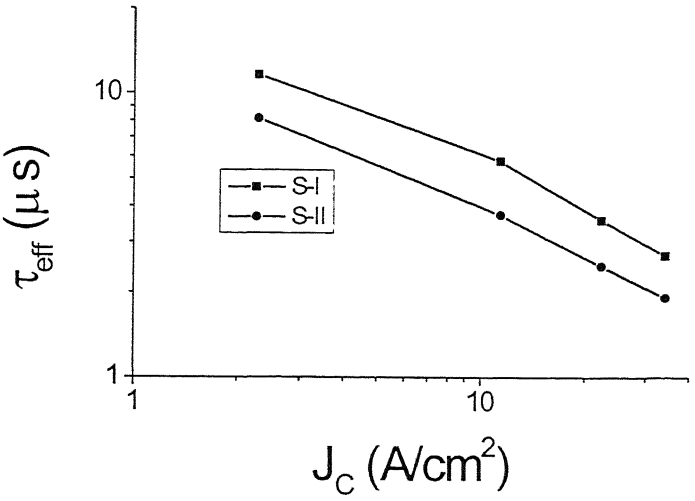


Fig. 3.16 τ_{eff} **vs** J_C **of high voltage transistors S-I and S-II**

As for the low voltage transistors, these results can be explained in terms of current ratio I_{hC}/I_B shown in Fig. 3.17.

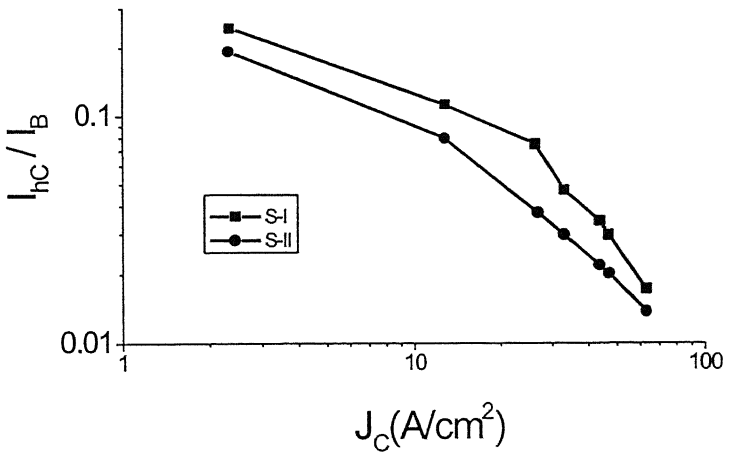


Fig. 3.17 I_{hC}/I_B **ratio vs** J_C **for high voltage transistors**

The ON state voltage at a current ratio of I_C/I_B equal to 2 for transistors S-I and S-II are shown in Fig. 3.18.

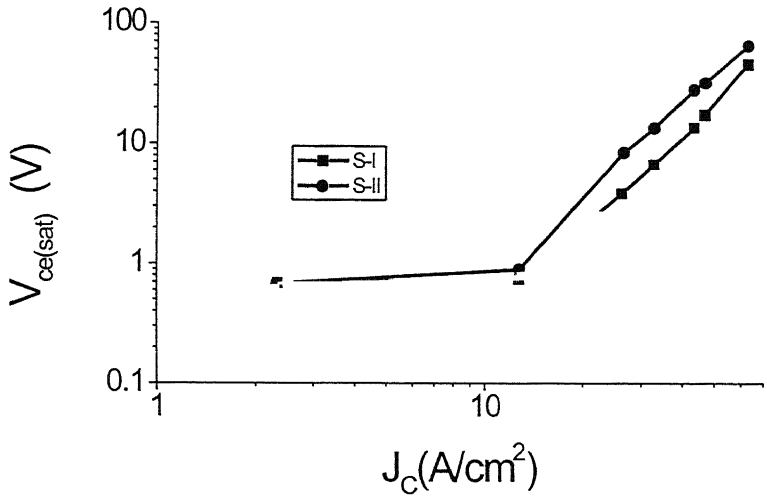


Fig. 3.18 Vce(sat) vs Jc for high voltage transistors, S-I and S-II

At low collector current densities, the ON state voltage for S-II is only marginally higher due to reduced reverse current gain. However, as collector current density increases, the ON state voltage begins to increase rapidly at a lower collector current for structure S-II. This result is in agreement with the predictions of the model Eq.(28-29) developed earlier. The reduction in hole injection into the collector results in formation of high resistance collector region at a lower collector current density in structure S-II. Although Eq. (28) is a highly simplified description of the transistor in saturation mode of operation, it fits the simulated data quite well for both the transistor structures. A plot of the ratio V_U/J_C with respect to I_{hC}/I_C in the region where collector-emitter voltage varies rapidly with collector current is shown in Fig. 3.19. The curves for both the

transistors are almost identical indicating that as the I_{hC}/I_C ratio decreases, the ratio V_U/J_C also increases.

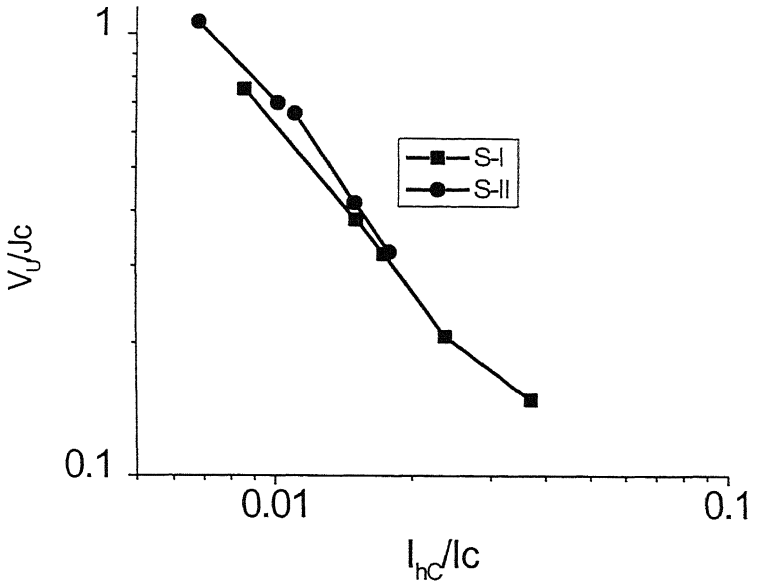


Fig. 3.19 **V_U/J_C vs I_{hC}/I_C**

To summarize, the results of 2D numerical simulations are in general agreement with the predictions of the analytical model and indicate that significant improvement in reverse recovery is possible through incorporation of universal contact in the extrinsic base region. However, this improvement is obtained at the expense of increased ON state voltage especially for transistors designed for high voltage operation at relatively higher collector current densities.

Apart from incorporating universal contact in the base, there is also a possibility of fabricating a structure in which a separate diode having universal contact, called Low Loss Diode (LLD), is integrated monolithically [2] along with the transistor in a manner similar to Schottky clamped transistor. This structure (Fig. 3.20), henceforth called S-III, is less efficient in reducing the effective minority carrier lifetime as compared to the structure S-II.

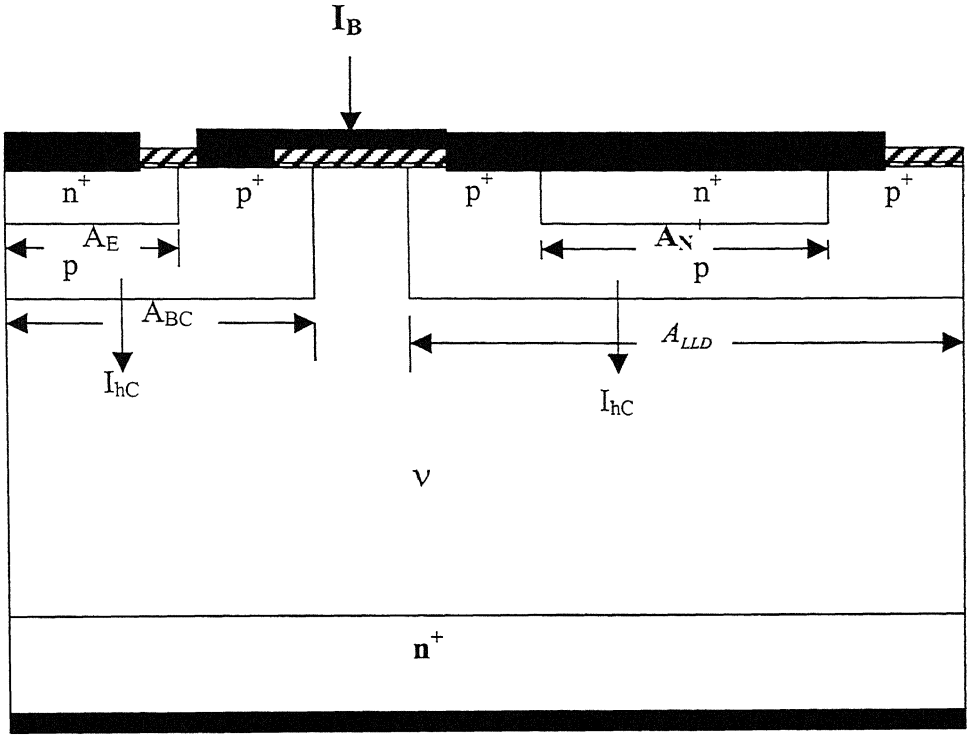


Fig. 3.20 Monolithic combination of LLD with transistor (S-III)

For both the structures, the effective minority carrier lifetime can be described by Eq.(3.8), which is reproduced again as:

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_o} + \frac{1}{\tau_{hBi}} + \frac{1}{\tau_{hBx}} \qquad (3.30)$$

To use Eq. 3.30 with transistor structure S-III, the externally connected low loss diode is viewed as an extension of the collector base area since it is electrically connected to it. A comparison of τ_{hBx} for the two structures gives an estimate of the relative efficiencies of the two structures. For structure S-III shown in Fig. 3.20, τ_{hBx}^{S-III} can be expressed using Eq. (3.7) as

$$\tau_{hBx}^{S-III} = \tau_0 \frac{A_{BC} + A_{LLD}}{A_{N^+}} \frac{J_{hC}^{S-III}}{J_{hBx}^{S-III}} \qquad (3.31)$$

Where A_N^+ is the area of n^+ region of the universal contact, which is taken to be the same in both S-II and S-III, A_{BC}, is collector–base area of S-III, also assumed to be the same as that for structures S-I and S-II and A_{LLD} is the area of LLD.

Similarly, for structure S-II

$$\tau_{hBx}^{S-II} = \tau_0 \frac{A_{BC} J_{hC}}{A_{N^+} J_{hBx}} \qquad (3.32)$$

Using the assumption that the injection efficiency of collector - base junction is the same for both structures, dividing Eq.3. 31 by Eq.3.32 give

$$\frac{\tau_{hBx}^{S-III}}{\tau_{hBx}^{S-II}} = \frac{A_{BC} + A_{LLD}}{A_{BC}} \qquad (3.33)$$

Eq. (3.33) shows that $\tau_{hBx}^{S-III} > \tau_{hBx}^{S-II}$ because when universal contact is introduced separately as in LLD, an additional region of area A_{LLD} has to be introduced which

besides increasing the electron injection in the external base region increases the hole injection into the collector also. This increases the effective lifetime in S-III.

Fig. 3.21 shows a comparison of reverse recovery waveforms obtained for structures S-II and S-III. The collector-base area of both the transistors was kept identical at 250 μm x 1 μm. In S-II, an N^+ region of area 80 μm x 1 μm was introduced in the extrinsic base region.

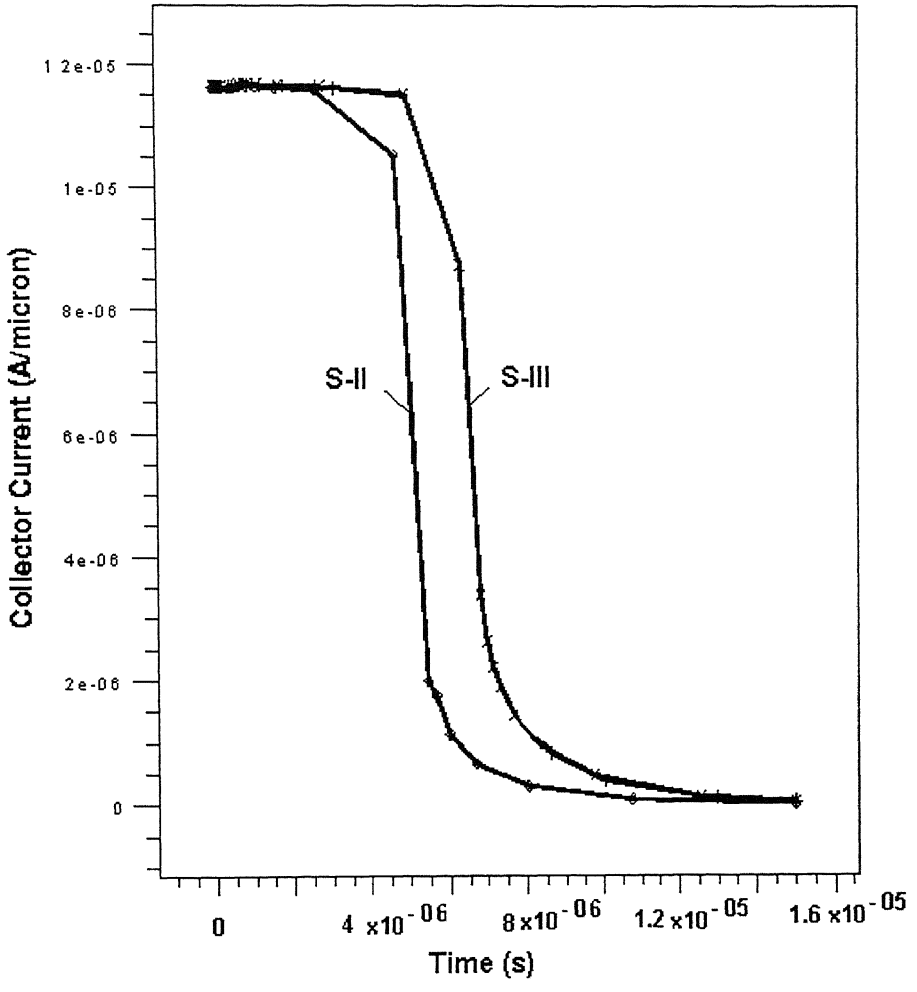


Fig. 3.21 Collector waveforms for structure S-II and S-III

In S-III, the area of LLD was taken as 190 μm x 1 μm with an n^+ region of area 80 μm x 1 μm, which is identical to that in S-II. To verify the above, two structures have been simulated for reverse recovery. The reverse recovery time of S-II is determined to be 33% lower than that of structure S-III. Substitution of area values in Eq. (3.32) shows that the effective lifetime of S-II is about 30.5% smaller than that for the structure S-III.

These results clearly show it is much more advantageous to introduce the universal contact inside the base of a transistor as in S-II rather than in the form of a low loss diode externally connected to it.

3.7 Experimental Results

Transistor structures S-I and S-II with two different breakdown voltages were fabricated and experimentally characterized. Table. 3.1 gives the doping and thickness of low voltage transistors that were fabricated using a four-mask process. The area of collector is 1.6 x 1.6 mm^2 and base area is 1.4 x 1.4 mm^2. The emitter has been diffused in finger like structure with area of 0.5606 mm^2. BJT S-II was also fabricated on the same chip by carrying out n^+ emitter diffusion in parts of the extrinsic base as well. In structure S-II, n^+ for making universal contact has been introduced in fine strips with total area of 0.33264 mm^2 and it covered approximately ¼ fraction of extrinsic base. The I_C-V_{CE} characteristics of both S-I and S-II were identical and are shown in Fig. 3.22.

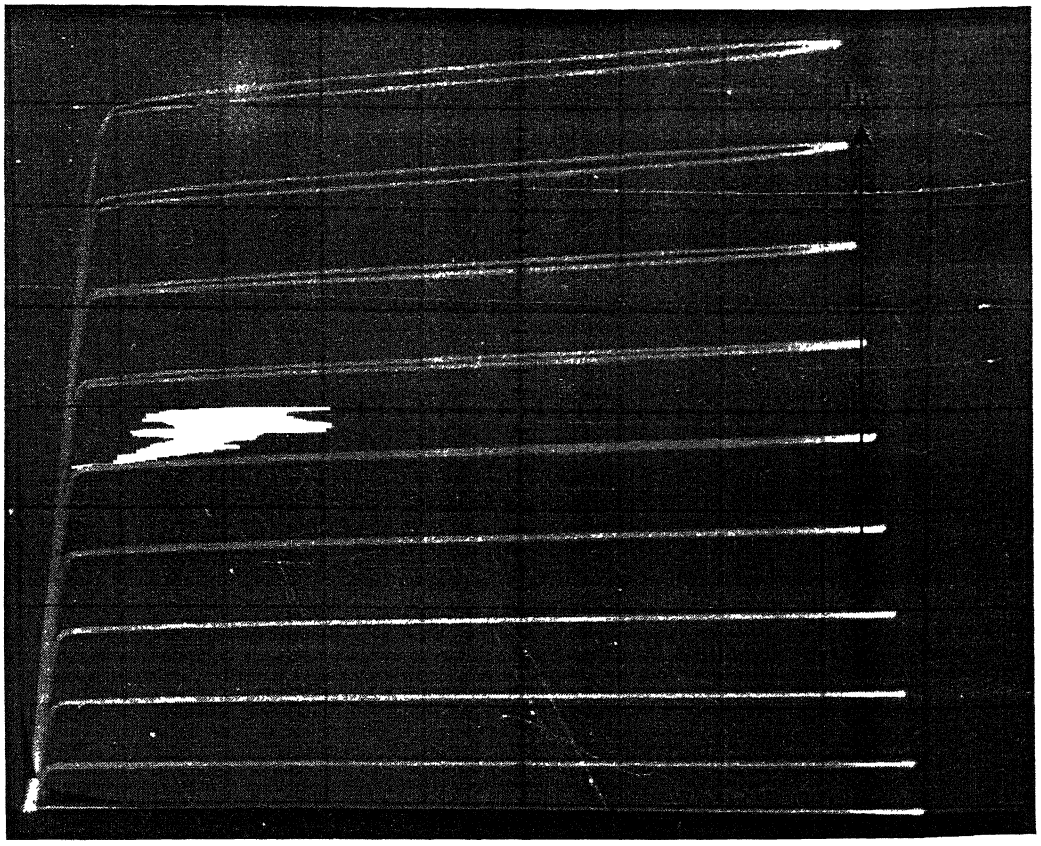
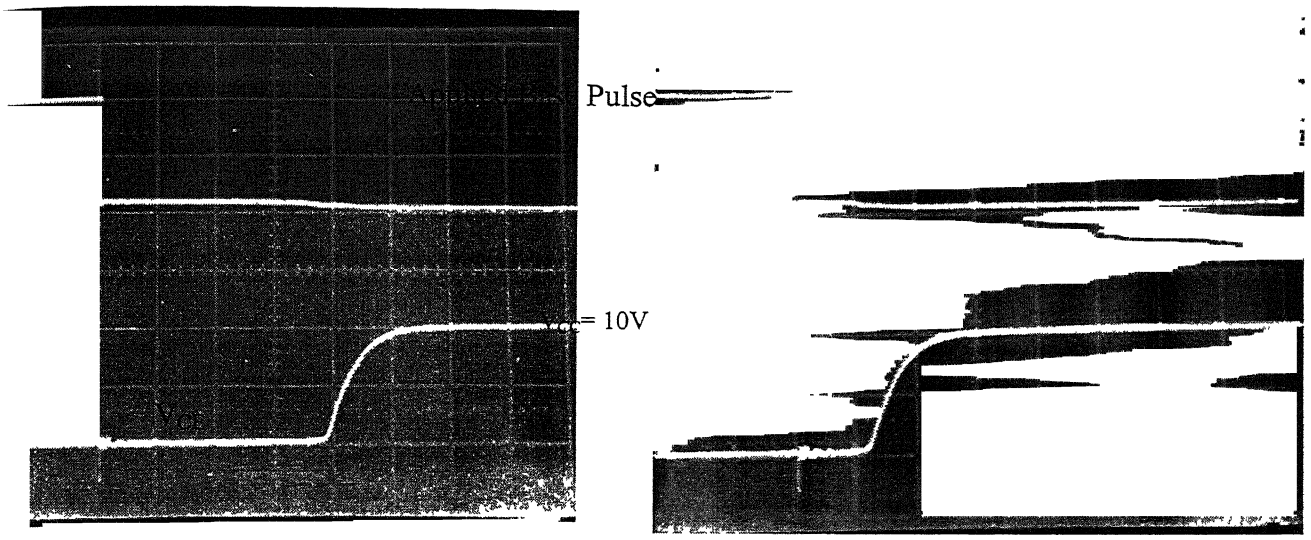


Fig.3. 22 **I_C-V_{CE} characteristics of experimental low voltage (BV_{CBO} ~ 150 V) transistor**

A current gain of 70 and identical breakdown voltages ranging between 100-155V were measured for both S-I and S-II. The reverse recovery measurements were carried out using a resistive load and abrupt switching of the base voltage. The reverse recovery waveforms for S-I and S-II are shown Fig. 3.23(a) & (b) respectively.



(a) (b)

Fig. 3.23 Photograph of measured reverse recovery of low voltage transistors (a) S-I (b) S-II (Hor. Scale 0.2 μs/Div, Ver. Scale 5 V/Div)

A reverse recovery time of 1 μs for S-I and 0.44 μs for S-II were obtained at a collector current of 20 mA. The 56% improvement in reverse recovery time is in fair agreement with simulation results considering the uncertainties due to factors such as collector recombination lifetime, Gummel charge under the extrinsic base etc used in simulation. The reverse recovery time for both S-I and S-II also improved with increase in collector current density. For example, values of reverse recovery of 0.5 μs at 10 mA and 0.38 μs at 40 mA were measured for S-II. The reverse recovery for few other collector current values are shown in Table 3.3.

Table 3.3 Measured dc & dynamic characteristics of experimental low voltage transistor

Device I.D	BV_{CBO} & leakage	Lifetime of collector with emitter open	β	I_C (mA)	Storage Time (μs)		Fall time (μs)		Total Recovery (μs)	
					S-I	S-II	S-I	S-II	S-I	S-II
W—12 (3x4)	BV 100-150 V, 0.1 μA at 50 V	2.6 μs	70	10 20 30 40	0.84 0.8 0.76 0.72	0.2 0.22 0.2 0.18	0.3 0.2 0.2 0.2	0.3 0.2 0.2 0.2	1.17 1.0 0.96 0.92	0.5 0.44 0.4 0.38

Measurement of $V_{CE(sat)}$ were carried out for different collector currents at a constant $\frac{I_C}{I_B}$=10. As can be seen from Fig. 3.24, the ON state voltage for S-II is higher as compared to S-I. As discussed earlier, at low currents, this is due to reduction in reverse current gain in S-II. The gain in reverse active mode was measured to be 8.8 and 1.8 for S-I and S-II respectively. Substitution of these numbers in Eq.(3.21) gives a difference of 28.6 mV in the ON state voltage of the two transistors.

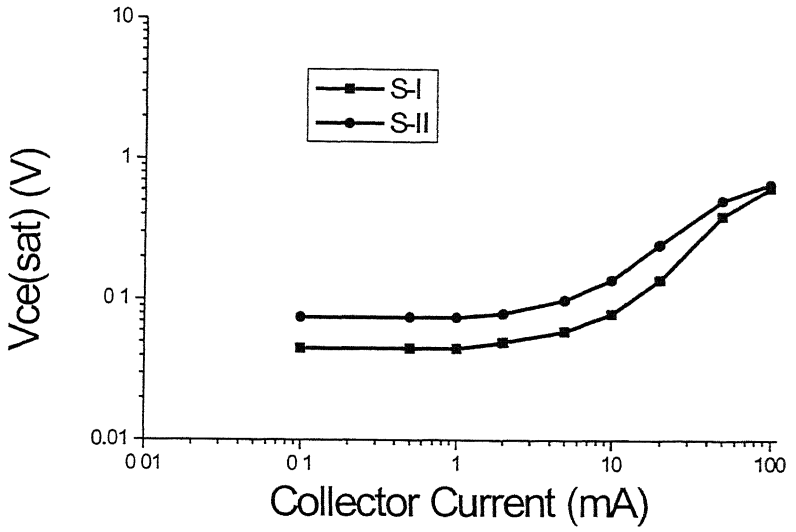


Fig. 3.24 **V_{CE}(sat) vs collector current at $\frac{I_C}{I_B}=10$ of low voltage transistor**

In order to measure the impact of universal contact in transistors of high breakdown voltages, devices with the description given in Table 3.2 were fabricated using a five-mask process details of which are given in Chapter IV. The area of collector is 3.4 x 3.4 mm^2 and that of base is 2.7 x 2.7 mm^2. The emitter has been diffused in finger like structure with area of 3.14 mm^2. BJT S-II was also fabricated along side by carrying out n^+ emitter diffusion in parts of the extrinsic base as well. In structure S-II, n^+ for making universal contact has been introduced in fine strips with total area of 1.1232 mm^2 and it covered approximately ¼ fraction of extrinsic base. The I_C-V_{CE} characteristics of structure are shown in Fig.3.25. A current gain ranging between 15-25 and identical breakdown voltages > 1000 were measured for S-I and S-II.

V_{CE} (V)

Fig. 3.25 **I_C-V_{CE} Characteristics of experimental high voltage (BV_{CBO} > 1000 V) transistor**

The reverse recovery measurements were carried out using a resistive load and abrupt switching of the base voltage. The reverse recovery waveforms for S-I and S-II are shown Fig.3.26 (a) & (b) respectively.

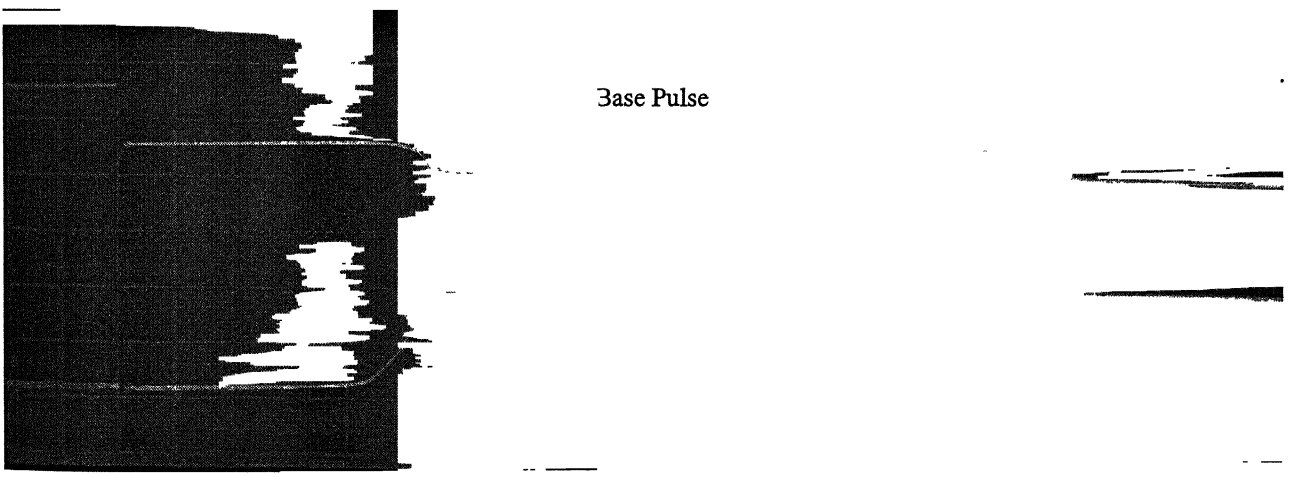


Fig. 3.26 **Photograph of measured reverse recovery of high voltage transistor (a) S-I (b) S-II (Hour. Scale 2 μs/Div, Ver. Scale 5 V/Div)**

A reverse recovery time of 10.4 μs for S-I and 8.4 μs for S-II were obtained at a forward collector current of 200 mA. The 23% improvement in reverse recovery time is in fair agreement with simulation results. The reverse recovery time for both S-I and S-II also improved with increase in collector current density. The reverse recoveries for few collector current values are shown in Table 3.4.

Table 3.4 Measured dc & dynamic characteristics of experimental high voltage transistor

Wafer I.D.	BV_{CBO}, Leakage	Life time in Collector	β	I_C ma	Storage Time (μs)		Fall time (μs)		Total Recovery (μs)	
					S-I	S-II	S-I	S-II	S-I	S-II
A3 — (2x 3)	> 1000 V, 10 μA at 1000 V	20 μs	15-25	100 200 300	12 8.4 6.2	8 6.4 5.2	3 2.0 1.6	4 0 2.0 1.6	15.0 10.4 7.8	12.0 8.4 6.8

Measurement of $V_{CE(sat)}$ were carried out for different collector currents at a constant $\frac{I_C}{I_B}=2$. As can be seen from Fig. 3.27, the on-state voltage for S-II is higher as compared to S-I. As discussed earlier, at low currents, this is due to reduction in reverse current gain in S-II. At high currents, it is due to the quasi-saturation as explained earlier.

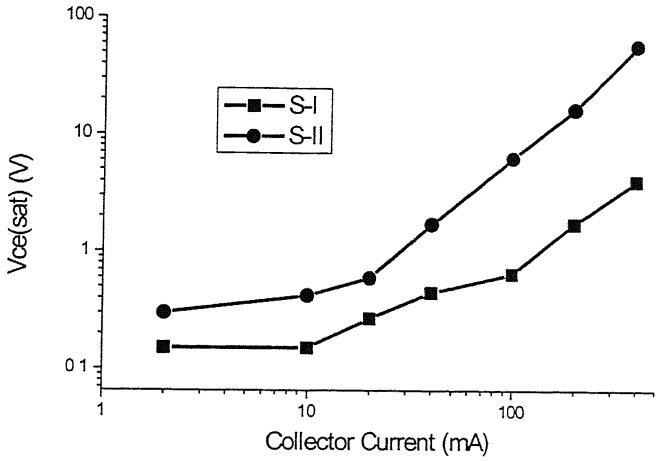


Fig. 3.27 **V_{CE}(sat) vs collector current at $\frac{I_C}{I_B}=2$ of high voltage transistor**

No measurable difference in breakdown voltage and leakage current was observed in low and high voltage transistors S-I and S-II.

3.8 SUMMARY OF BJT RESULTS

The use of "universal contact" for improving the reverse recovery of power bipolar transistor (BJT) was studied in detail using a combination of analytical model, numerical simulation and experimental work. It is shown that use of universal contact allows redistribution of base current in saturation from collector region where recombination lifetime is high to extrinsic base region where effective recombination lifetime is low. The analytic model also predicts that the effective lifetime is inversely proportional to the current density. It is also shown through analysis that the efficacy of

the universal contact in reducing the effective lifetime becomes less as the breakdown voltage of the transistor increases. The improvement in reverse recovery is accompanied by degradation of the ON state voltage. For low voltage, the degradation is solely due to reduction in current gain in reverse active mode while for high voltage transistor, the degradation is characterized by an early onset of quasi-saturation effect.

CHAPTER IV

DEVICE TECHNOLOGY

In this work, we fabricated diodes and transistors, conventional and the ones having universal contact adopting identical processes. The voltage rating of these devices is approximately same as the devices, which have been simulated in previous sections. The material, technology and process flow of the fabricated diodes and transistors is described in following sections.

4.1 RAW MATERIAL

The reverse voltage capability of the diode and transistor is the sole factor for deciding the resistivity and width of the raw material. The current rating depends upon the length of the emitter periphery and can be increased by proper design of fingers, cells or area of the device. To study the universal contact in low (~150) and high voltage (~1000V) devices, the following materials were obtained:

For a 150V devices	nn^+ Epitaxial
	Resistivity 3.4 – 4.6 Ω-cm
	Phosphorous doped Epi thickness 15 μ m
	Substrate (Sb doped), Resistivity 0.015 Ω-cm
	Substrate thickness 310 ± 20 μ m
Supplier	Wacker-Chemitronic GmbH, German

For > 1000V devices	Phosphorous doped bulk FZ grown silicon
	Resistivity 100 Ω-cm
	Initial thickness 350 ± 10 μm
Supplier	Wacker-Chemitronic GmbH, German

4.2 DIODE FABRICATION

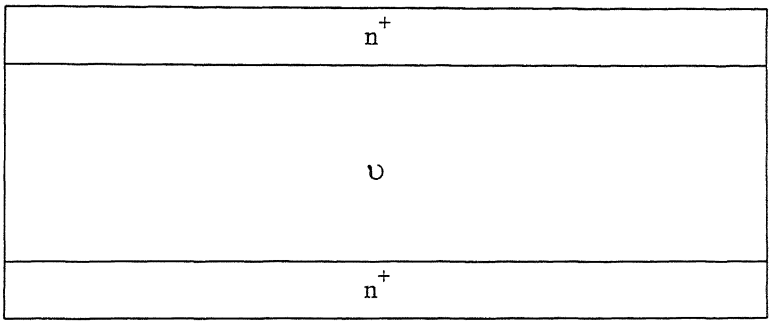
The four-mask process was developed for planar low voltage diode. First mask for p^+ window open, second mask for n^+ UC, third mask for contact open and fourth one for aluminum metal patterning. An additional mask for moat etching was required for high voltage diode. All masks were locally designed and developed. The base area is 1.4 x 1.4 mm^2 for planar structure. The actual base area of mesa etched devices is reduced to 1.1 x 1.1 mm^2. The conventional diode (S-I) and diode incorporating universal contact (S-III) has been made in the same wafer as to reduce the material and process variations. The p^+ diffusion was done using boron doped oxide by Chemical Vapor Deposition (CVD)[31] using tri-propyle-borate and tetra-ethyle-orthosilicate (TEOS) by pyrolytic decomposition at 660°C. It was followed by soak-in, removal of doped oxide and drive-in to obtain the required surface concentration and junction depth. In last step, the n^+ diffusion was done using $POCl_3$ from back and front. This last high temperature step getters the metallic impurities besides introducing the n^+ doping required for universal contact. In high voltage devices, the curved portion of the p diffusion gives rise to high

electric field near the surface, which may cause ionic drift. This affects the reliability of the device. To overcome this, the curved portion producing the high surface field is chemically etched. Out of the different technique [32] for lowering the surface electric field, the mesa etching, which is compatible with batch process has been used. To passivate the junction, the mesa has been filled with a special glass, GP-601 from Nippon Electric Glass (NEG). A paste of the glass with Ethyl Cellulose and Butyl Carbitol is made which is then filled in mesa grooves by doctor blading. The glass was fired in oxygen in a suitable glass firing cycle. Al evaporation was done in 3-4 x 10^{-6} mbar range on the front side, patterned and sintered at 450-500°C. The Ti-Au was done on the backside of the wafer. The four-probe setup was used for sheet resistivity measurement. The junction depth was measured using lapping and staining with copper nitrate. The process flow is given as under:

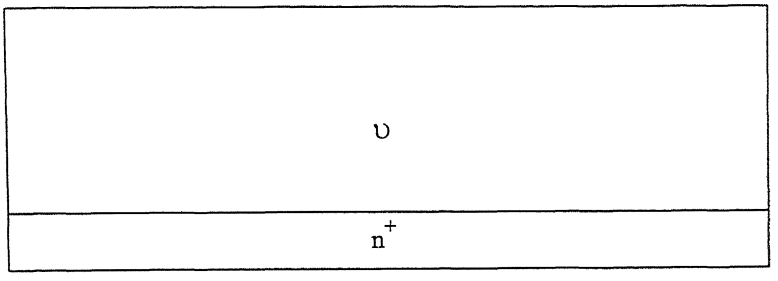
Pre-processing of Epitaxial wafers (3.4 –4.6 Ω-cm) using TCA oxidation, 4 hrs, 1170°C, O_2 1 lpm, TCA 75 ml/m

Pre-processing of bulk wafers (100 Ω-cm) to remove point defects and metallic impurities using , $POCl_3$ gettering at 1050°C, 1 hr, Rs. 1.4 -1.6 Ω/sq, Etching of few μm silicon from both sides and TCA oxidation, 6hrs 1170°C, O_2 1 lpm, TCA 75 ml/m

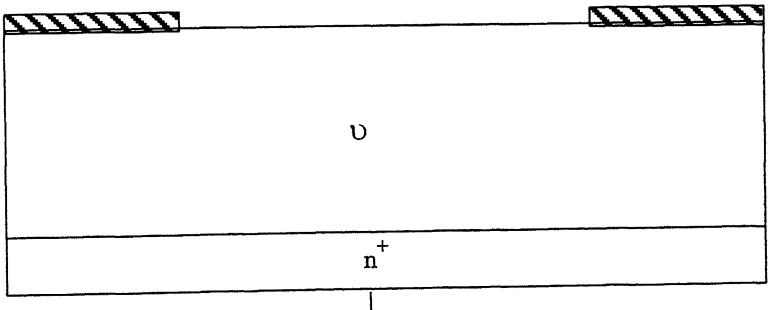
n^+ deposition on both sides of bulk wafer of 100 Ω-cm and 30 hrs drive-in at 1225°C in oxygen and TCA ambient. Rs 5.6 – 18.8 Ω/sq, xj 30-35 μm.



Removal of n^+ from one side, using lapping and polishing



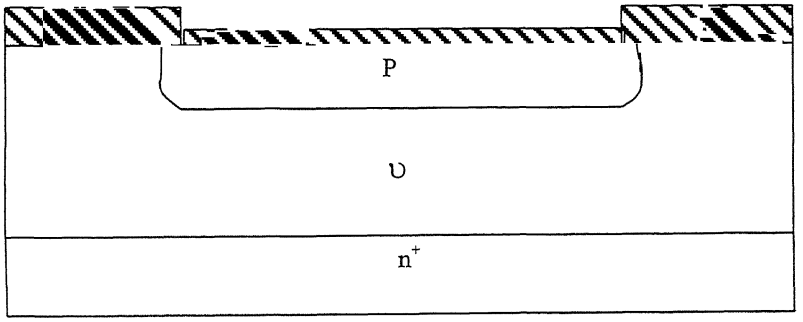
Oxidation, Photolithography for Ist mask for p^+ window open.



Oxide

Boron deposition and drive-in 1200°C 4 hrs in oxygen & TCA ambient, Rs = 98.0 Ω/sq, xj = 5.44 μm for low voltage diode/transistor.

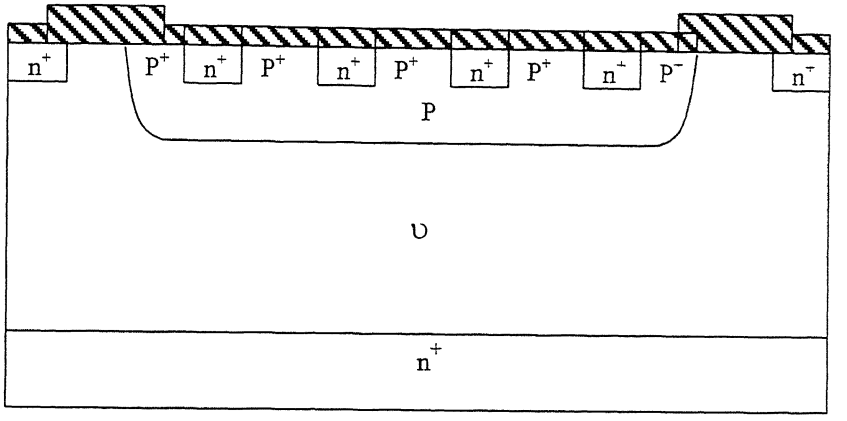
Boron deposition, soak-in and drive-in at 1240°C 28 hrs in oxygen & TCA ambient, Rs = 100 Ω/sq., xj = 23 μm for high voltage diode/transistor



Oxide

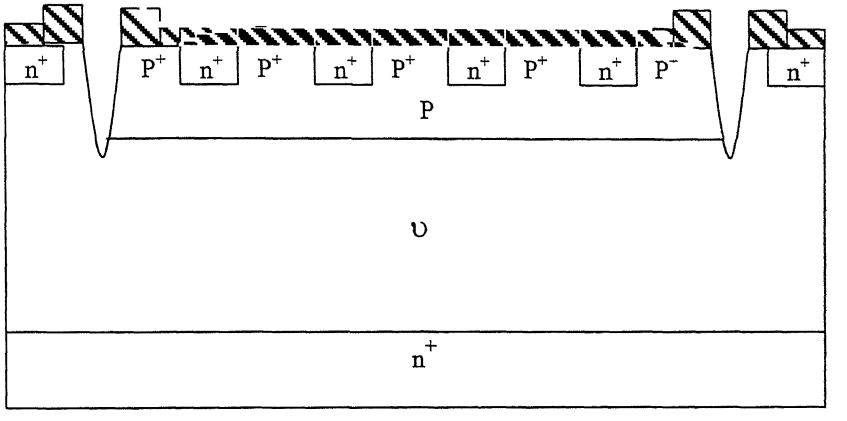
Photolithography for IInd mask for n^+ & $POCl_3$ deposition at 1000°C, 25 min, Drive-in at 1100°C, 1 hrs, Rs=1.8 Ω/sq, xj= 3.2 μm in oxygen ambient for Low Voltage diode/transistor

Photolithography for IInd mask for n^+ & $POCl_3$ deposition at 1050°C, ½ hrs. Drive-in at 1100°C, 6 hrs, in oxygen ambient, Rs=5.6 Ω/sq, xj= 7 μm for high voltage diode/ transistor



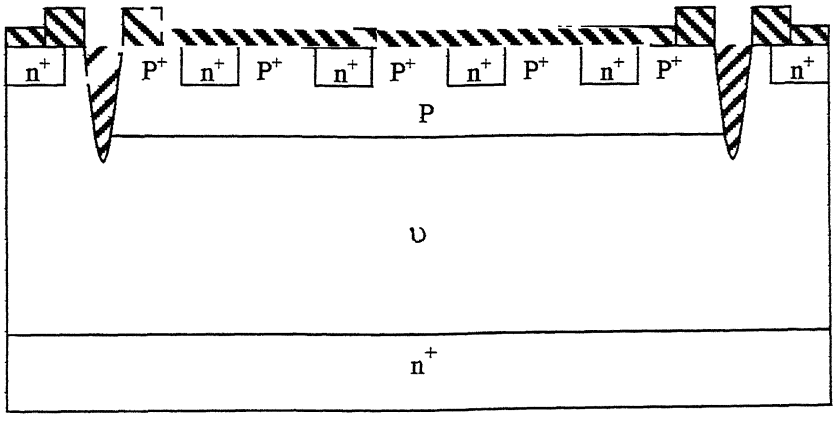
Oxide

Moat etching 40-50 μm using 5:3:3::HnO_3:HF:Acetic Acid
Using IIIrd mask



Oxide

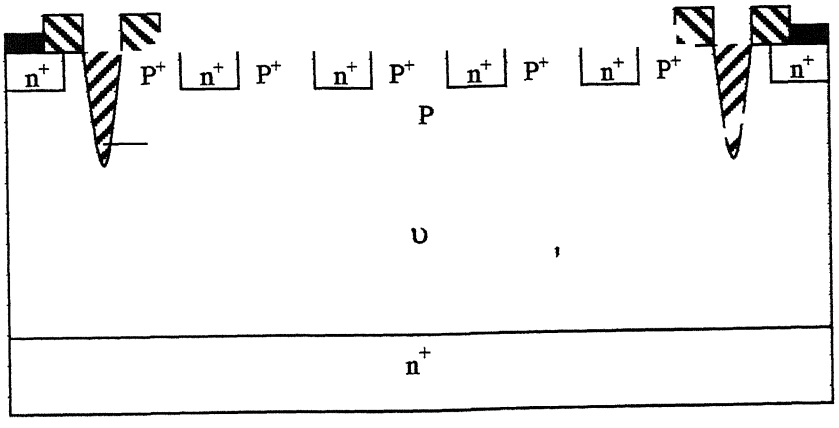
Glass (NEG GP-601) filling using doctor blading and firing the glass according to specified cycle



Oxide

Glass

Front Al metallization and patterning using Vth mask

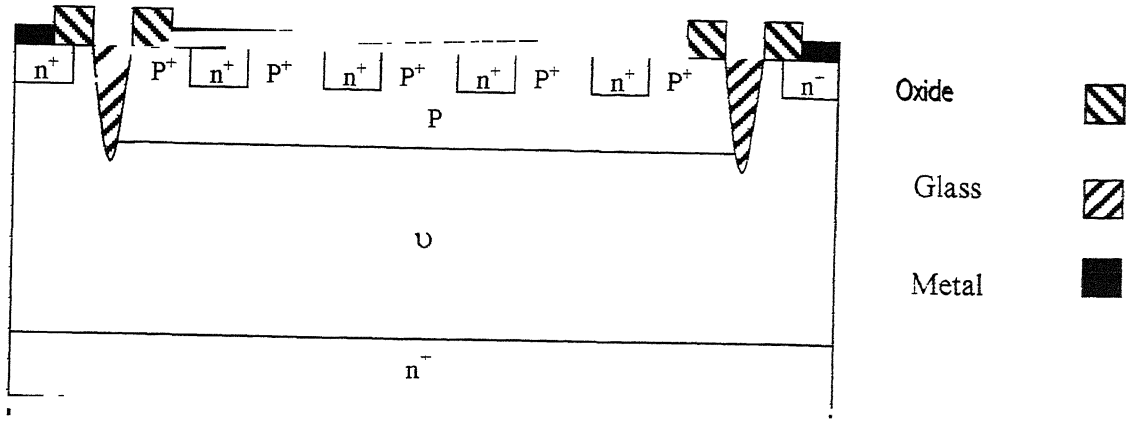


Oxide

Glass

Metal

Back Ti-Au Metallization



The photographs of the finished die of conventional diode and the one having n^+ nd p^+ ratio of 1:1, 2:1 and 4:1 for making the universal contact are shown in Fig. 4.1.

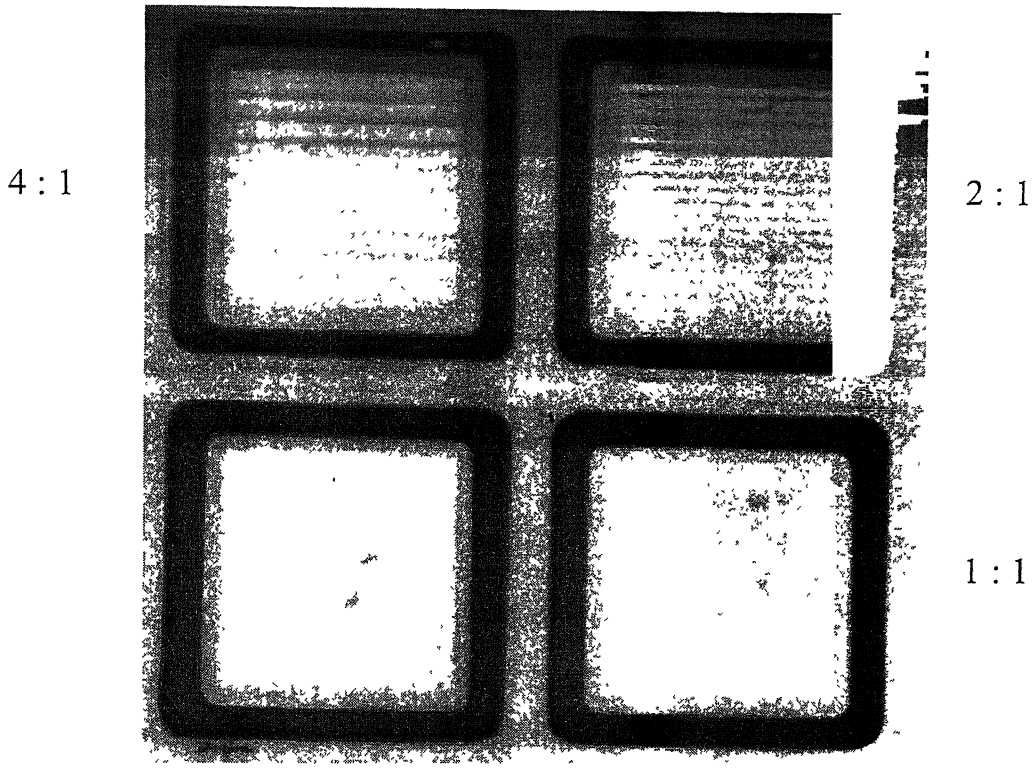


Fig. 4.1 Photograph of conventional (S-I) and modified (S-III) diodes

The high voltage diode structure incorporating universal contact at the end of high resistivity region has also been fabricated. There is about 35 μm n^- diffused region on right side of a power diode made in bulk silicon. This n^- diffused region has been etched away and n^+ p^+ contact has been made in its place. This structure in essence becomes equal to the diode structure S-II shown in Fig. 2.3.

4.3 TRANSISTOR FABRICATION

4.3.1 LOW VOLTAGE TRANSISTOR

Similar to diodes, the fabrication of low voltage planar transistor required four masks process. First mask for p^+ window open, second mask for emitter and n^+ UC, third mask for contact open and fourth one for aluminum metal patterning. All masks were locally designed and developed. The base area is 1.4 x 1.4 mm^2 for planar low voltage transistors. The conventional low voltage transistor (S-I) and the transistor incorporating universal contact (S-II) has been made in the same wafer as to reduce the material and process variations. The emitter layout has been designed using inter-digitated emitter-base finger geometry. The emitter finger width is 100 μm and that of base finger is 80 μm. The n^+ p^+ universal contact has been applied with 1:1 ratio in base fingers. However, the device has additional extrinsic base area for metal pad. In this area too, universal contact has been applied. The n^+ diffusion for making the universal contact has been made at the time of emitter diffusion.

The enlarged photograph of the fully processed low voltage planar transistor is shown in Fig. 4.2.

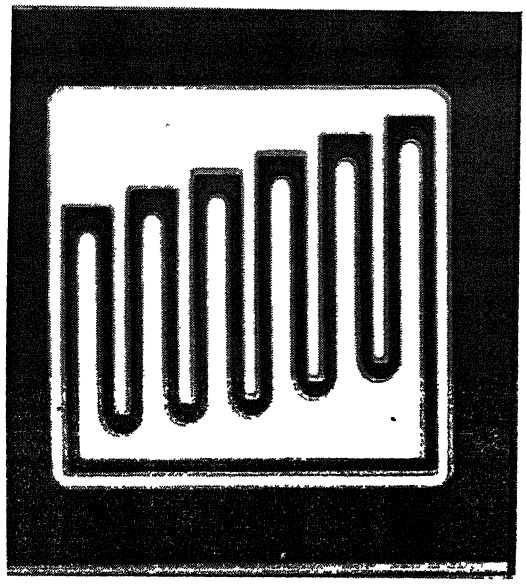


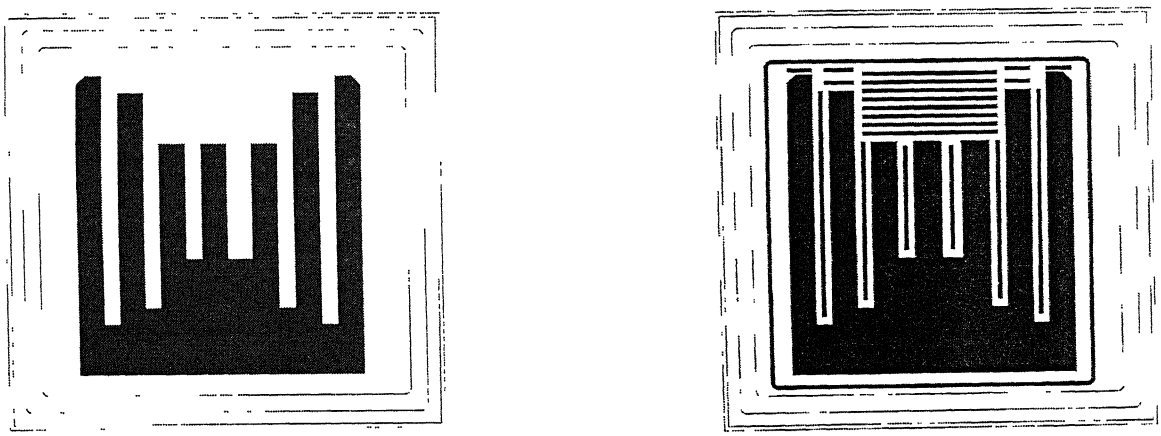
Fig. 4.2 Photograph of the low voltage conventional planar transistor

4.3.2 High Voltage Transistor

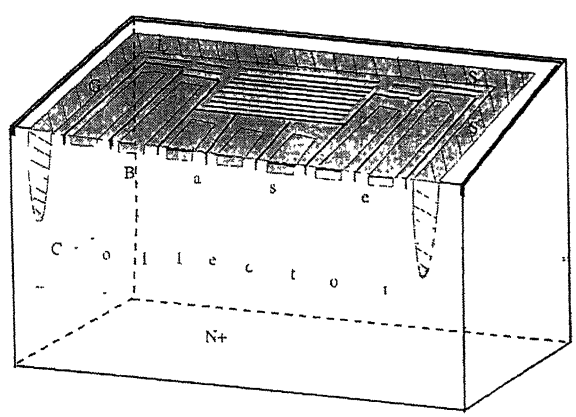
The fabrication of high voltage transistor required five-mask process. First mask for p^+ window open, second mask for emitter and n^+ "universal contact", third mask for contact open, fourth mask for moat etching and fifth mask for aluminum metal patterning. All masks were locally designed and developed. The high voltage transistor is different from its low voltage counterpart. The main concern in high voltage transistor is to reduce the ON state voltage. To operate device at high currents and low ON forward voltage, recourse is usually made to increase the device area. The high voltage transistor

have been fabricated in chip size 3.5 X 3.5 mm^2 die of BV_{CBO} ~ 1500 V and current rating of ~ 5 A. The emitter finger width is 200 μm and base finger width is 150 μm.

The process flow for low and high transistor is similar to the one adopted for low and high voltage diodes respectively. The top views of high voltage transistors S-I and S-II are shown in Fig. 4.3 (a) and (b). 3-D view of S-II is shown in Fig.4.3(c).



(a) (b)



POWER BJT (MODIFIED) - CROSS SECTION

(c)

Fig. 4.3 **(a) Top view of conventional (S-I) transistor, (b) Top view of modified (S-II) transistor, (c) 3-D view of S-II**

A photograph of fully processed die of conventional high voltage BJT is shown in Fig. 4.4. The modified transistor S-II has also been made in the same batch. The n^+p^+ universal contact has been introduced in extrinsic base similar to the top view shown in Fig.4.3(b).

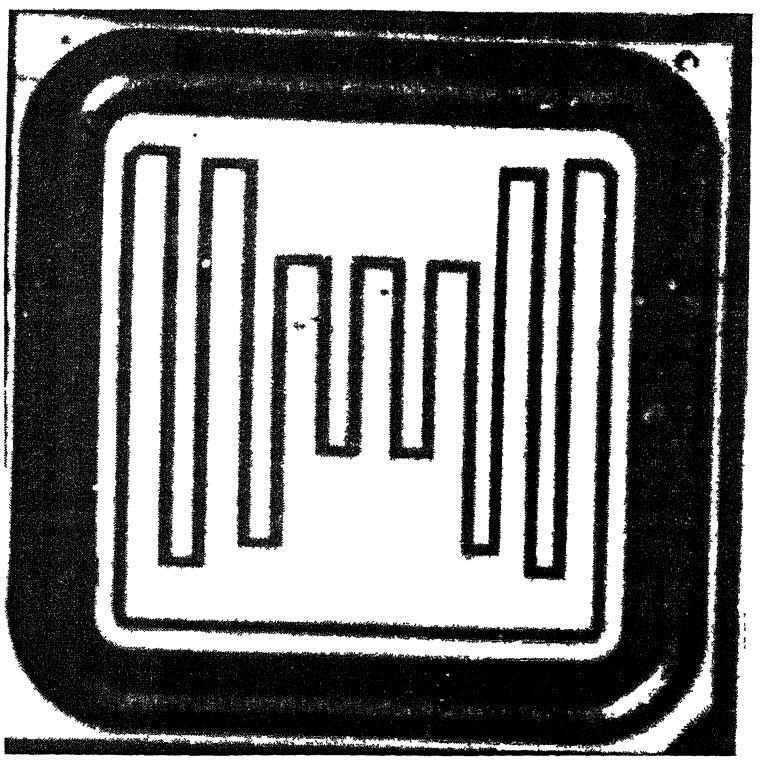


Fig. 4.4 Photograph of the high voltage conventional transistor

4.4 GROWN IN DEFECTS AND YIELD PROBLEMS

The main difficulty faced in the development of these devices was the quality of the raw material. For low voltage diodes and transistors, epitaxial wafers have been used.

The FZ silicon bulk wafers have been used for high voltage devices. The hyper pure quality wafers were procured from a world-renowned manufacturer. The devices made in the raw wafers in the first few runs had large leakage current. There was almost no visible sharp breakdown voltage. The $POCl_3$ gettering [33, 34] was not enough to remove these defects. To find the cause of the low breakdown and large leakage, an investigation of raw and processed wafers was carried out. During preferential etching, large number of tiny defects distributed in swirl pattern were observed in raw wafers. These defects pointed to the presence of silicon point defects either excess self-interstitial or vacancies. The excess interstitial may nucleate at defect sites and act as recombination centers, causing large leakage. The Electron Probe Microanalysis (EPMA) revealed that there were trace amounts of metallic impurities present in the bulk of the wafer.

To remove these metallic impurities, gettering at higher concentration of $POCl_3$ and longer time was carried out. No improvement was observed in leakage current and breakdown. It was found during these gettering experiments that the excessive $POCl_3$ gettering rather spoiled the wafers further. The $POCl_3$ treatment though helpful in removing the metallic impurities, introduces excess silicon interstitial. The CZ or FZ methods of pulling the crystal invariably introduce some impurities and grown-in point defects [35, 36]. The kind and concentration of point defects in silicon wafer depends on its growth conditions. The parameter s defined as growth rate (v) / temperature gradient (G) [37] during crystal growth decides whether it will have excess interstitial or vacancies.

The excess interstitial in the wafer can be removed by treating them at high temperature in chlorine containing ambient. The chlorine introduces excess vacancies at the surface of the wafer [38], which induces diffusion towards the surface of the silicon atoms sitting in silicon precipitates. The silicon precipitates are thus dissolved and removed from the bulk of the wafer by chlorine treatment. Keeping the effects of the chlorine containing ambient and that of the $POCl_3$ in view, a wafer cleaning process was optimized. For creating chlorine ambient, 1-1-1 trichloroethan (TCA) was bubbled through by passing N_2 in it. The process details for 100 Ω-cm bulk wafers are given in the flow chart. The epitaxial wafers were also subjected to mild TCA treatment. The devices with low leakage and high breakdown were ultimately obtained.

CHAPTER V
CONCLUSIONS

The objectives of this thesis has been to study the reduction of reverse recovery in low and high voltage diodes and bipolar transistors by the incorporation of universal contact and its effects on other device characteristics. The conclusions drawn from the present work are summarized below.

5.1 DIODE

1. The use of n^+p^+ "universal contact" for improving the switching performance of power diodes was examined in detail through modeling of effective minority carrier lifetime (τ_{eff}). It was shown that τ_{eff} depends not only on the lifetime in the lightly doped v region but also on other time constants determined by the fraction of total current that results from the injection of minority currents into p^+ and n^+ region. Using this viewpoint, it is shown that effective minority carrier lifetime and therefore reverse recovery time which is closely related to it, can be reduced by redistributing current away from lightly doped v-region to n^+ and p^+ regions where effective minority carrier lifetime can be reduced by incorporating universal contact. It was found that the incorporation of

this modification in p^+ improved the effective lifetime of low voltage diodes (100 –200 V) by 68% at 100 A/cm^2 and for high voltage (1000 V) diode by 39% at about 50 A/cm^2. The corresponding improvement in effective lifetime in high voltage diode structure as proposed by Amemiya et al is 43% but this structure compromised the breakdown voltage which is reduced to less than half of the conventional high voltage diode

2. The analytical model developed in this work shows that the effective lifetime decreases with increase in current density and that the advantages of incorporating a universal contact decrease as the breakdown voltage of the diode increases. Due to the large middle region thickness in high voltage diodes, the fraction of current injected into p^+ region is relatively less and the improvement of reverse recovery is also less as compared to low voltage diodes. The reverse recovery time for both low and high voltage diodes was found to decrease with current density. This is due to the difference in voltage dependence of current injected into the p^+ region (ideality factor ~ 1) and the middle ν region (ideality factor ~ 2). It is also shown that the incorporation of universal contact allows a new tradeoff between the switching speed and the reverse blocking voltage determined by the proximity of universal contact to the lightly doped region of the diode. The predictions of the model were verified through extensive 2-D [4] numerical simulation and fabrication and characterization of low (~150 V) and high (>1000 V) voltage diodes.

3. A new diode structure incorporating universal contacts inside both n^- and p^+ diffused regions has been proposed. It was shown through analytical calculations and 2D numerical simulations that this diode structure results in large reduction in reverse recovery. The improvements in reverse recovery are 60% and 66% at 0.3 A/cm^2 and 50 A/cm^2 respectively with respect to the conventional diode structure. It is further shown that the ON state voltage of the proposed structure is smaller than that of the conventional diode structure by 145 mV at about 50 A/cm^2. [39]

5.2 TRANSISTOR

4. The use of "universal contact" for improving the reverse recovery of power bipolar transistor (BJT) was studied in detail using a combination of analytical model, numerical simulation and experimental work. The analytical model developed for PIN diodes was extended to model the effects of incorporating universal contact within the extrinsic base of BJTs. It is shown that use of universal contact allows redistribution of base current in saturation from collector region where recombination lifetime is high to extrinsic base region where effective recombination lifetime is low. The analytic model also predicts that the effective lifetime is inversely proportional to the current density. The numerical simulation results show that effective lifetime decreases from 849 ns at 1 A/cm^2 to

88 ns at about 110 A/cm^2. It is also shown through analysis that the efficacy of the universal contact in reducing the effective lifetime becomes less as the breakdown voltage of the transistor increases. There is about 50-70% improvement in reverse recovery in low voltage transistor by incorporating the universal contact. This improvement is only 20-35% in high voltage transistor.

5. The improvement in switching characteristics as a result of incorporation of universal contact is accompanied with an increase in the ON state voltage, $V_{CE(sat)}$ of transistors. For low voltage device, there is about 30-50 mV increase in $V_{CE\ (sat)}$ due to reduction in current gain in reverse active mode in transistors incorporating UC. In high voltage transistor, the increase in $V_{CE(sat)}$ in transistors with universal contact at high current density is in the order of few volts due to early onset of quasi-saturation effect. These results are verified through 2-D numerical simulation and fabrication and characterization of low voltage (BV_{CBO} ~ 150 V) and high voltage (BV_{CBO} >1000 V) transistors.

6. The usefulness of the universal contact at high voltage (BV_{CBO} >1000 V) transistors has been experimentally demonstrated for the first time. An improvement of 23% in reverse recovery was experimentally measured in high voltage BJT [40].

7 It is much more advantageous to introduce the "universal contact" inside the base of a transistor rather than in the form of a low loss diode (LLD) externally connected to it [2,14].

TABLE 'A' OPTIMUM DRIFT REGION WIDTH AND DOPING FOR DESIRED BREAKDOWN VOLTAGE

Width (μm)	Back Ground Concentration (/cm^3)	Desired Breakdown (V)		
		Parallel Plane	Planar (50%)	Mesa Etched (80%)
5	9.5e14	131	65.5	-
10	5e14	237	118.5	-
18	2.5e14	393	196.5	-
20	2e14	430	215.0	-
30	1.3e14	609	304.5	-
40	9.0e13	780	390.0	623
50	7.0e13	944	472.0	755
60	5.5e13	1104	502.0	882
70	5.0e13	1260	630.0	1008
80	4.0e13	1413	706.5	1130
100	3.0e13	1710	-	1368
110	2.9e13	1856	-	1485
120	2.6e13	2000	-	1600
130	2.4e13	2142	-	1713
140	2.2e13	2282	-	1826
150	2.0e13	2421	-	1937
160	1.9e13	2559	-	2047
170	1.7e13	2696	-	2156
180	1.6e13	2830	-	2264
190	1.5e13	2965	-	2372
200	1.4e13	3098	-	2478

DEVICE SIMULATION SOFTWARE TOOLS

Many software packages like MEDICI[41], ATLAS[15] and BIPOLE [42] are commercially utilized for the simulation and optimization of the various device parameters before manufacturing them The simulation package [15] has been utilized for the 2-D simulation done in the present work. It consists of the following modules.

DevEdit

It is an interactive tool for specifying and modifying device structure. It includes a meshing module that supports mesh generation, refinement, and un-refinement. It uses triangular mesh. Base material, doping profile types their type, doping etc. may be defined and modified using analytical functions. It can be used as a stand-alone tool or it can be invoked by DeckBuild. Large devices with many grids points may be specified completely using DevEdit making this tool valuable as a preprocessor for 2D Device simulations. DevEdit3 supports the definition and meshing of 3D structures. We have license for 2D simulation for the present.

ATLAS is a physically based two and three-dimensional device simulator. It predicts the electrical behavior of specified semiconductor structures, and provides insight into the internal physical mechanisms associated with device operation. Semiconductor device operation is modeled in ATLAS by a set of anywhere from one to six coupled, non-linear, partial differential equations (PDEs). ATLAS produces numerical solutions of these equations by calculating the values of unknowns on a mesh of points within the device. An internal discretization procedure converts the original, continuous model to a discrete non-linear algebraic system that has approximately the same behavior. The set of PDEs, the mesh and the discretization procedure determine the non-linear algebraic problem that must be solved. The non-linear algebraic system is solved using an iterative, Newton, Gummel or Block or any combination of it, procedure that refines successive estimates of the solution. Iteration continues until the corrections are small enough to satisfy convergence criteria, or until it is clear that the procedure is not going to converge. The non-linear iteration procedure starts from an initial guess. The corrections are calculated by solving linearized versions of the problem. The linear sub-problems are solved by using direct techniques or iteratively.

In transient simulation, the carrier continuity equations are integrated in the time domain. Time integration schemes differ in their accuracy, in the number of previous time levels they employ, and in their stability properties. For drift-diffusion calculations, ATLAS uses a composite of trapezoidal rule (TR) - Backward Difference Formula-2 (BDF2) scheme that was developed by Bank et.al [43]. This method is one-step, second

order and both A-stable and L-stable. An estimate of local truncation error (LTE) is obtained at each time step, and this estimate is used to automatically adapt the time step.

The order in which statements occur in an ATLAS input file is important. There are five groups of statements, and these must occur in the correct order. The failure to do so usually causes an error message and termination of the program

1.	Structure Specification	MESH
		REGION
		ELECTRODE
		DOPING
2.	Material Models Specification	MATERIAL
		MODELS
		CONTACT
		INTERFACE
3.	Numerical Method	METHOD
4.	Solution Specification	LOG
		SOLVE
		LOAD
		SAVE

DeckBuild

ATLAS is normally used through the DeckBuild run-time environment that supports both interactive and batch-mode operation. The input files can be directly entered once the Deckbuild is started. DeckBuild Command Menu can help to create input files. It can be configured for different default modules. The Command Menu gives access to pop-up windows in which desired information is typed. When "Write" button is selected, syntactically correct statements are written to the DeckBuild text edit region. It covers most of the possible ATLAS syntax. The run-time output shows the execution of each ATLAS command and includes error messages, warning, extracted parameters and other important output for evaluating each ATLAS run.

Tonyplot

It is a Visualization Tool, which provides comprehensive interactive scientific visualization capabilities. All of the usual ways of displaying scientific data are supported by it and we can get hard copy of plots.

The above modules provide the general framework of the simulator. There are different modules, which supports different material and analysis capabilities. For silicon, S-PISCES is used. GIGA provides the non-isothermal calculations. Mixedmode provides

the device based circuit simulation capabilities. BLAZE for III-V compounds, TFT for poly-silicon based devices, LUMINOUS for opto-elctronic devices, LASER for hetro-structures, DEVICE3D for three dimensional device simulation. Besides, the general framework of the simulator as described above; we have license only for S-PISCES and GIGA.

We have carried out different static I-V experiments and reverse recovery experiments using the above. The input files have been written in the Deckbuild editor window.

LIFETIME MEASUREMENT USING OPEN CIRCUIT VOLTAGE DECAY (OCVD)

The operating principle and circuit are given in [43]. To the first order, the effective recombination lifetime is given by

$$\tau_{eff} = \frac{n\frac{kT}{q}}{\frac{dV}{dt}}$$

Where n varies 1 to 2 from low to high injection conditions. The τ_{eff} is an effective lifetime influenced by emitter recombination, back surface recombination for short-base diodes, edge effects and process conditions. The following circuit was rigged to measure the lifetime using Open Circuit Voltage Decay (OCVD).

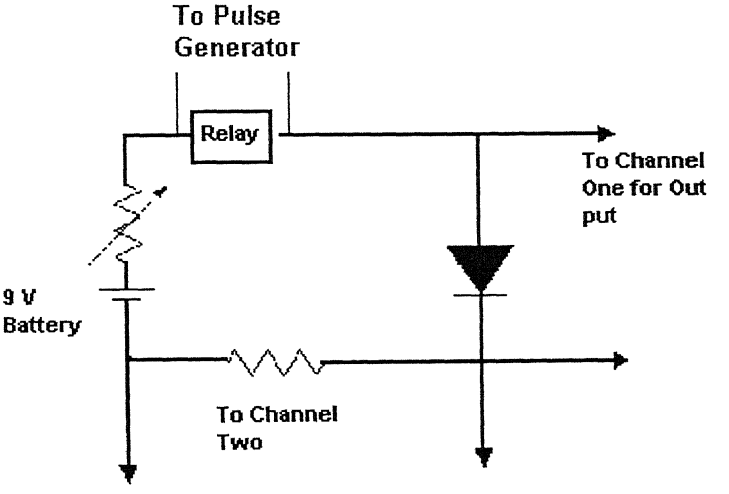


Fig. (C.1) Experimental setup for measuring Lifetime using Open Circuit Voltage Decay (OCVD)

Table C – Change of Lifetime of PIN Diode with Current

Current (mA)	Small Area (1 mm^2)		Large Area (25 mm^2)	
	Current Density (A/cm^2)	Lifetime (μs)	Current Density (A/cm^2)	Lifetime (μs)
1	0.1	26	0.004	115
10	1.0	17.3	0.04	104
70	7.0	14.8	0.28	86

The above result show that lifetime depends on area. Also as seen from above Table 'C' and shown by [44], the effective lifetime also depends upon current levels. The lifetime of the experimental diode and transistor were therefore measured at low current density using the above circuit.

EXPERIMENTAL MEASUREMENTS

Numbers of measurements were made in diodes and transistors. Static characteristics like leakage current, breakdown voltage, V_{CE} and β were measured using curve tracer. Reverse recovery including the storage and fall time effects were measured using reverse recovery method. These values are given in chapters II and III under subsection of Experimental Results.

EXPERIMENTAL SETUP TO MEASURE THE REVERSE RECOVERY OF DIODES

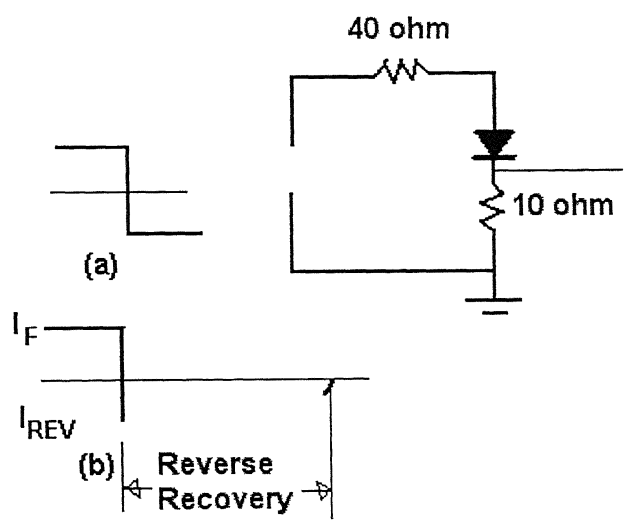


Fig. D.1 Experimental circuit for reverse recovery measurement of diodes

The circuit as shown in Fig (D.1) was rigged-up. Forward and reverse drive currents were kept same. The applied pulse and response of the diode are shown in Fig. D.1.

EXPERIMENTAL SETUP - TRANSISTORS

The circuit as shown in Fig. D.2 was rigged-up. A base drive pulse wide enough to saturate the device was applied

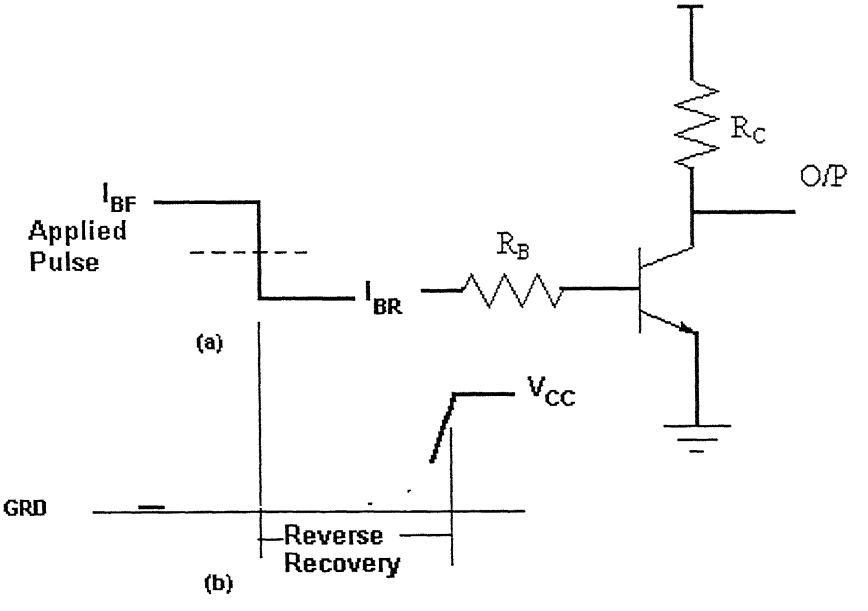


Fig. D.2 **Experimental circuit for reverse recovery measurement of transistors.**

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